Welcome To

ISSCC 2014
Session 2
Ultra-High-Speed Wireline Transceivers and Techniques

28Gb/s 560mW Multi-Standard SerDes with Single Stage Analog-Front End and 14-tap Decision Feedback Equalizer in 28nm CMOS

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Outline

- Motivation
- Architecture
- Circuit Design
  - AFE, DFE and Clock buffer
- Measurement results
- Conclusions

Motivation

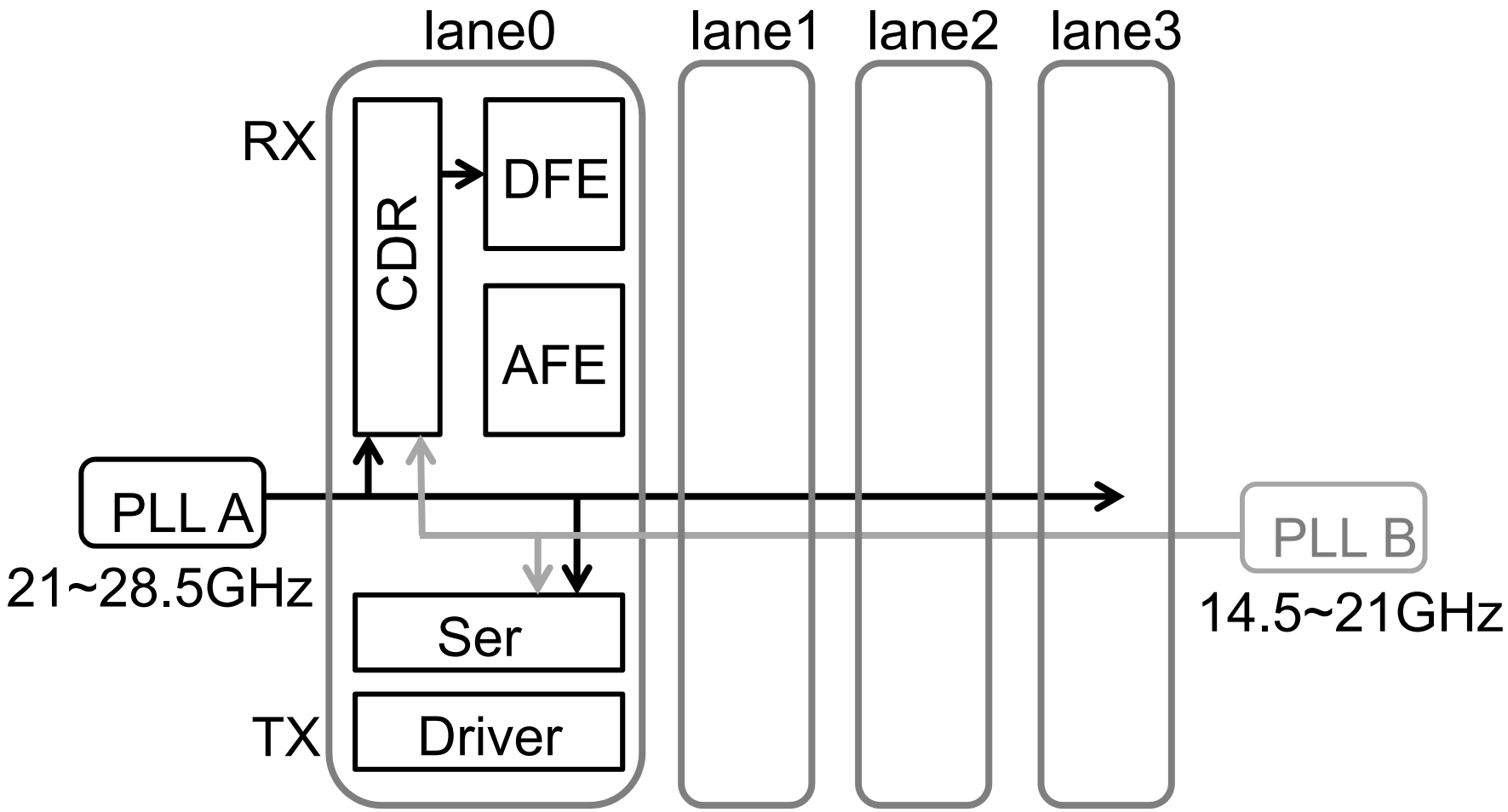
- **New Standards require 25~28Gbps data rate**
  OIF CEI-25G-LR, CEI-28G-MR/SR/VSR, IEEE802.3bj and 32G-FC

- **High Speed Serdes challenges**
  -High speed operation
  -Low power consumption
  -Small die area
  -Intensive equalization
  -Robustness

- **Needs for new circuit topology and system architecture**

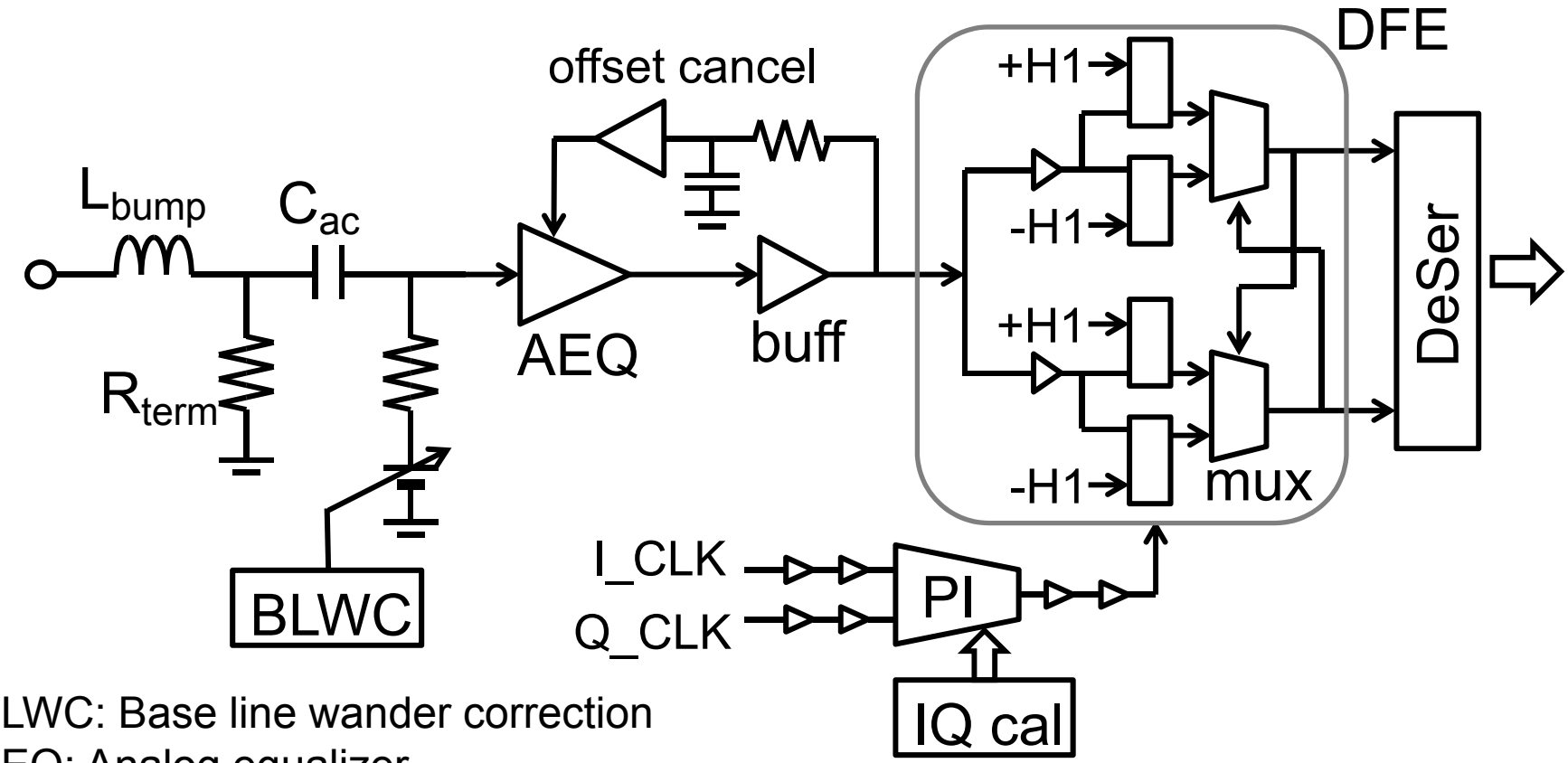
Serdes Subsystem Architecture

- Cover multi-standards with 14.5-28.5Gb/s native rate
- Support rate agility on lane basis with dual PLLs and independent clock muxs



RX Block Diagram

- On-chip AC coupled with BLWC
- Intensive equalization: AEQ of 15dB boost + 14 tap DFE
- PI based CDR with UI/64 resolution

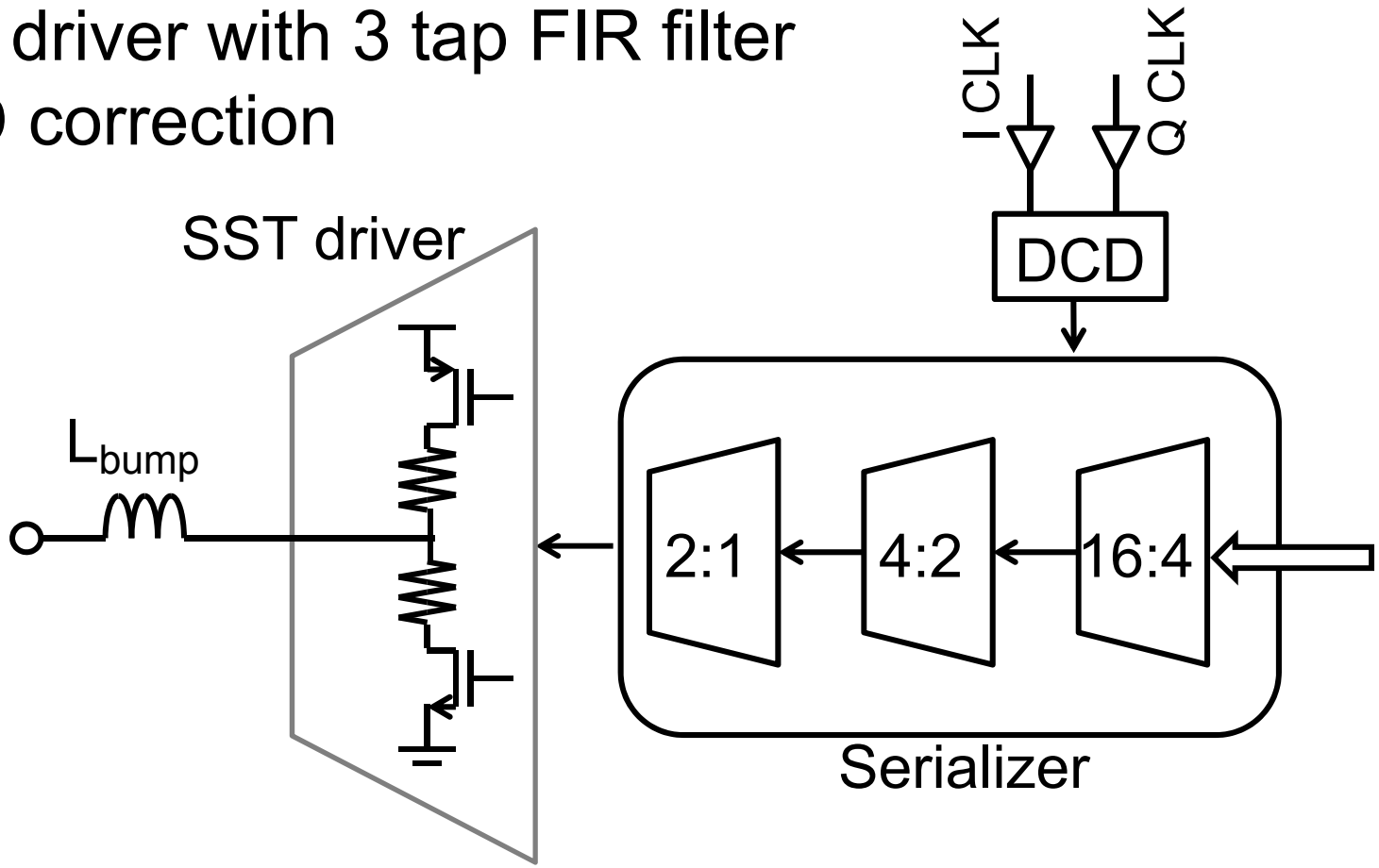


BLWC: Base line wander correction
AEQ: Analog equalizer
PI: Phase interpolator

UI: Unit interval

TX Block Diagram

- SST driver with 3 tap FIR filter
- DCD correction



SST: Source series terminated
DCD: Duty cycle distortion

Reference : F. Zhong, et al.,JSSC, no.12. 2011

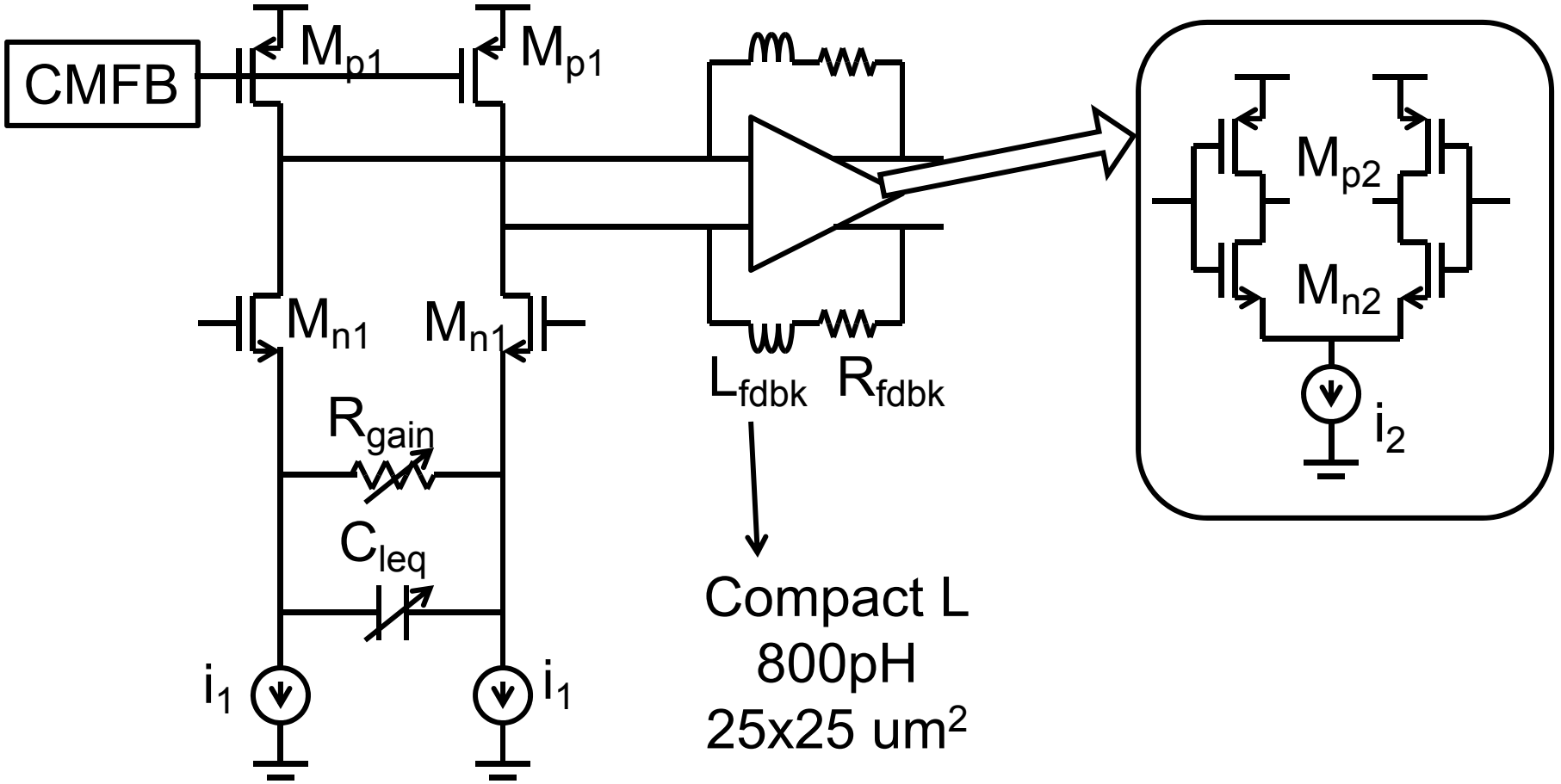
Analog Front-end Challenge

- **High bandwidth, large high frequency boost & linearity**
- **Low Power**
- **Robustness**

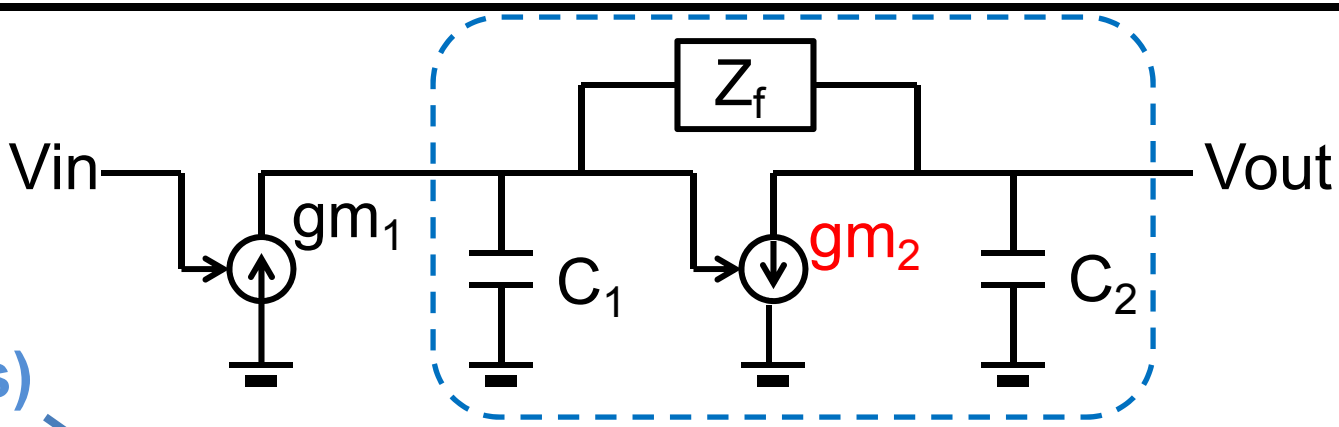
- **Minimum number of stage for Robustness and BW**
- **Trans-impedance amplifier(TIA) structure for high bandwidth**
- **Compact inductor for high frequency boost**

AFE Circuit Diagram

- VGA+LEQ in single stage
- TIA to improve bandwidth



TIA Transfer Function



TIA(s)

$$\frac{Vout}{Vin} = gm_1 \frac{\frac{1}{C_1 C_2 Z_f}(1 - Z_f gm_2)}{s^2 + \frac{C_1 + C_2}{C_1 C_2 Z_f} s + \frac{gm_2}{C_1 C_2 Z_f}}$$

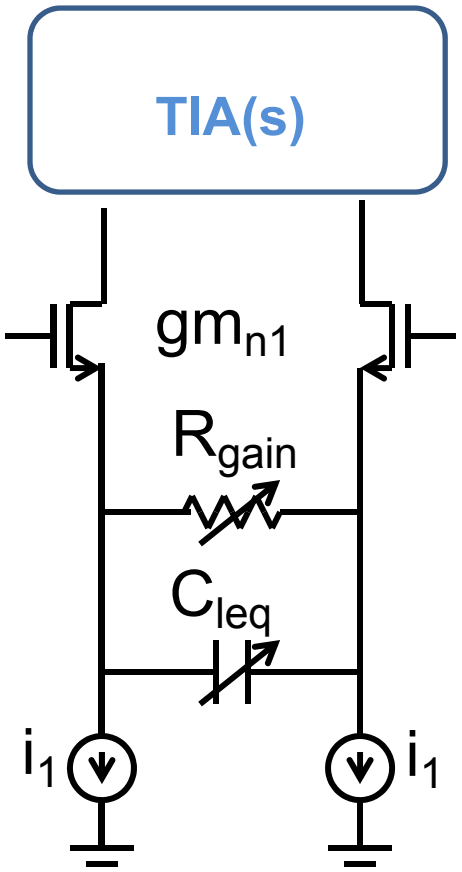
$$\omega p = \sqrt{\frac{gm_2}{C_1 C_2 Z_f}}$$

$$dc\_gain = -gm_1\left(Z_f - \frac{1}{gm_2}\right)$$

$$Q = \frac{\sqrt{gm_2 C_1 C_2 Z_f}}{C_1 + C_2}$$

- With large gm_2, improve high frequency behavior
- dc_gain is simplified to $gm_1 Z_f$

Transfer Function of TIA-based AFE



Overall AFE transfer function is expressed by diff-pair with TIA loading.

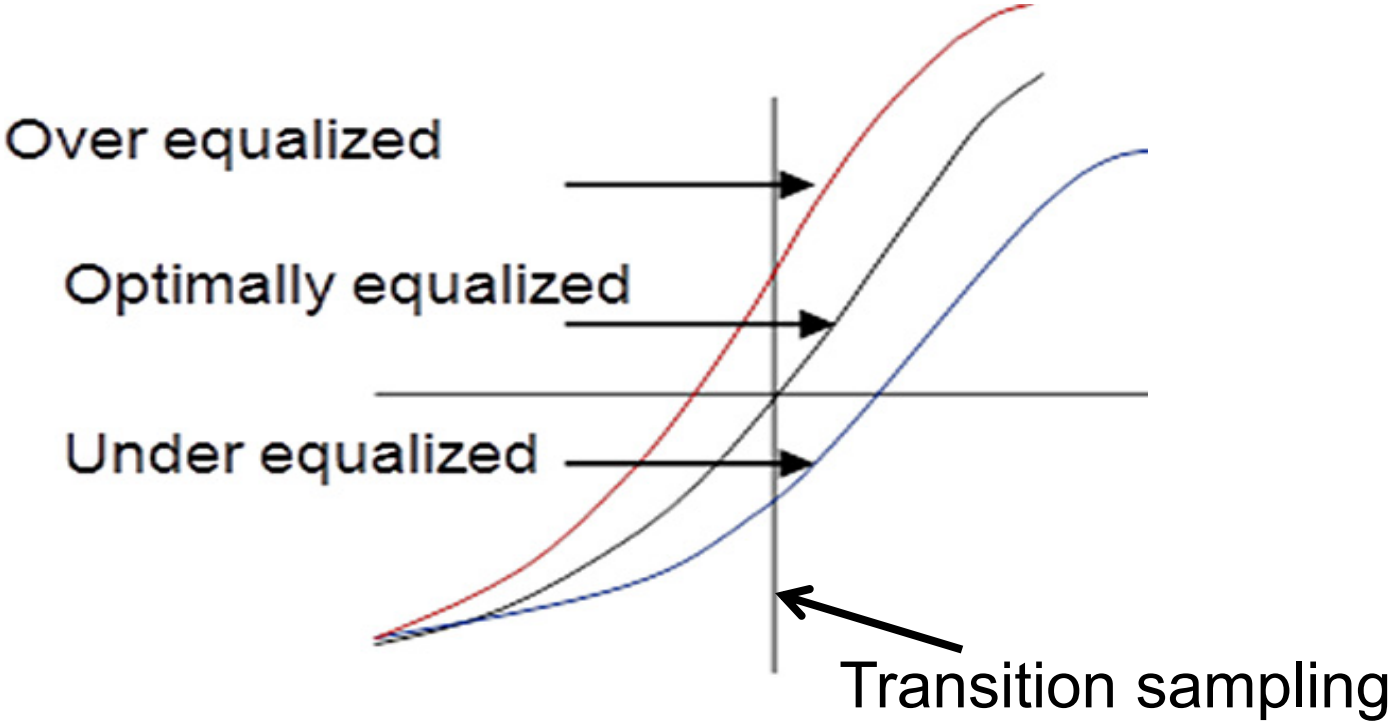
$$\frac{Vout}{Vin} = \frac{gm_{n1}\,(1 + s\,C_{leq}\,R_{gain})}{s\,C_{leq}\,R_{gain} + 1 + gm_{n1}\,R_{gain}}\,TIA(s)$$

$$dc\_gain = \frac{1}{R_{gain} + 1/gm_{n1}}\left(Z_f - \frac{1}{gm_2}\right)$$

$$zero = \frac{1}{C_{leq}\,R_{gain}}$$

- Gain is controlled by R_{gain}
- Boost is controlled by C_{leq}

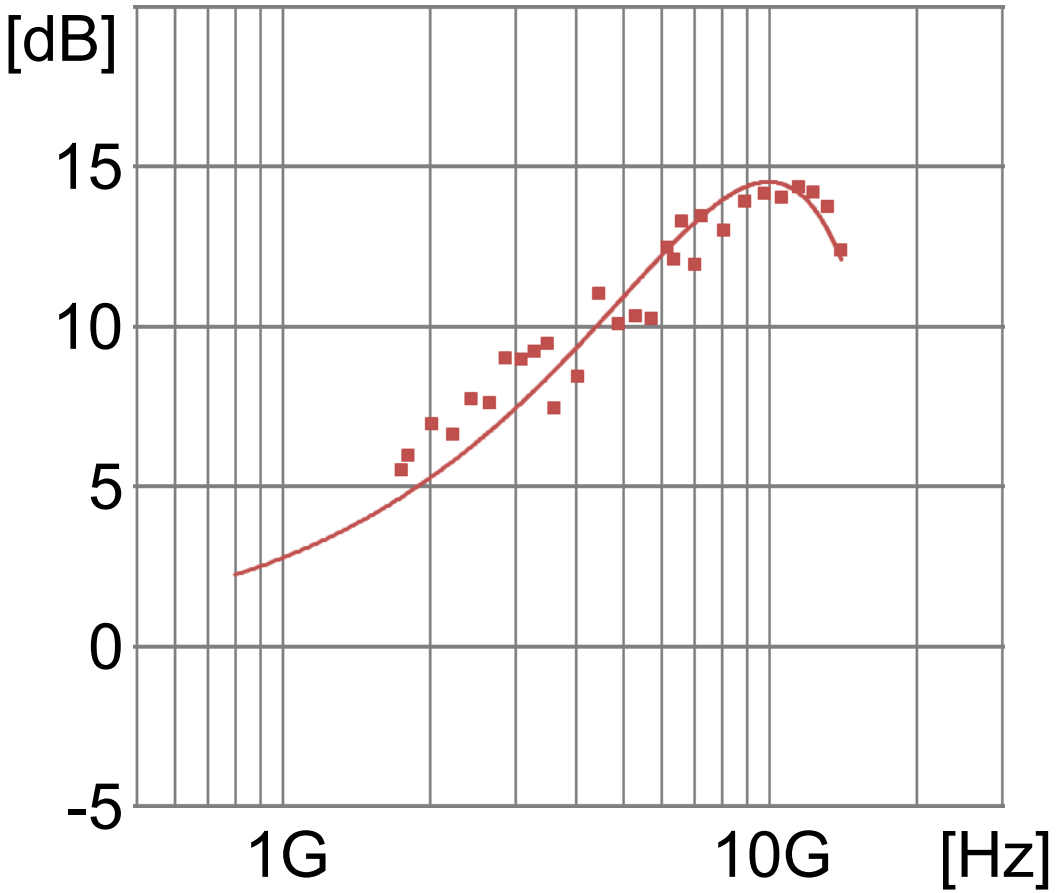
Group Delay Adaptation Algorithm



- AFE peaking is adapted by relating the sliced transition sample with the sliced data samples
- Group delay algorithm eliminates potential coupling with DFE adaptation

Digitally Measured AFE Frequency Response

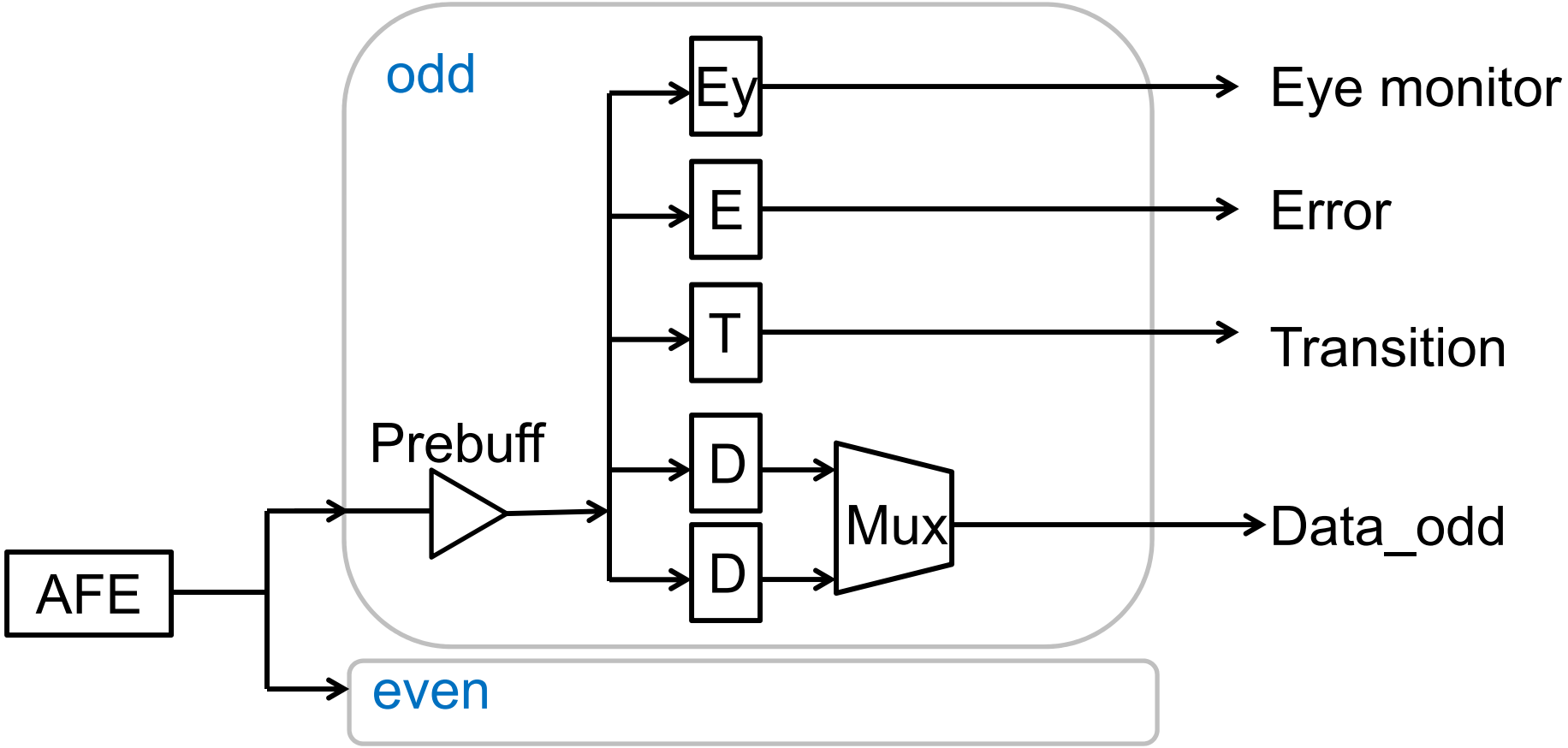
1. Apply sinusoidal wave and sweep the freq.
2. CDR to lock to signal and run adaptation without DFE.
3. Monitor the mean target amplitude from H0.
4. Calc the gain from H0.



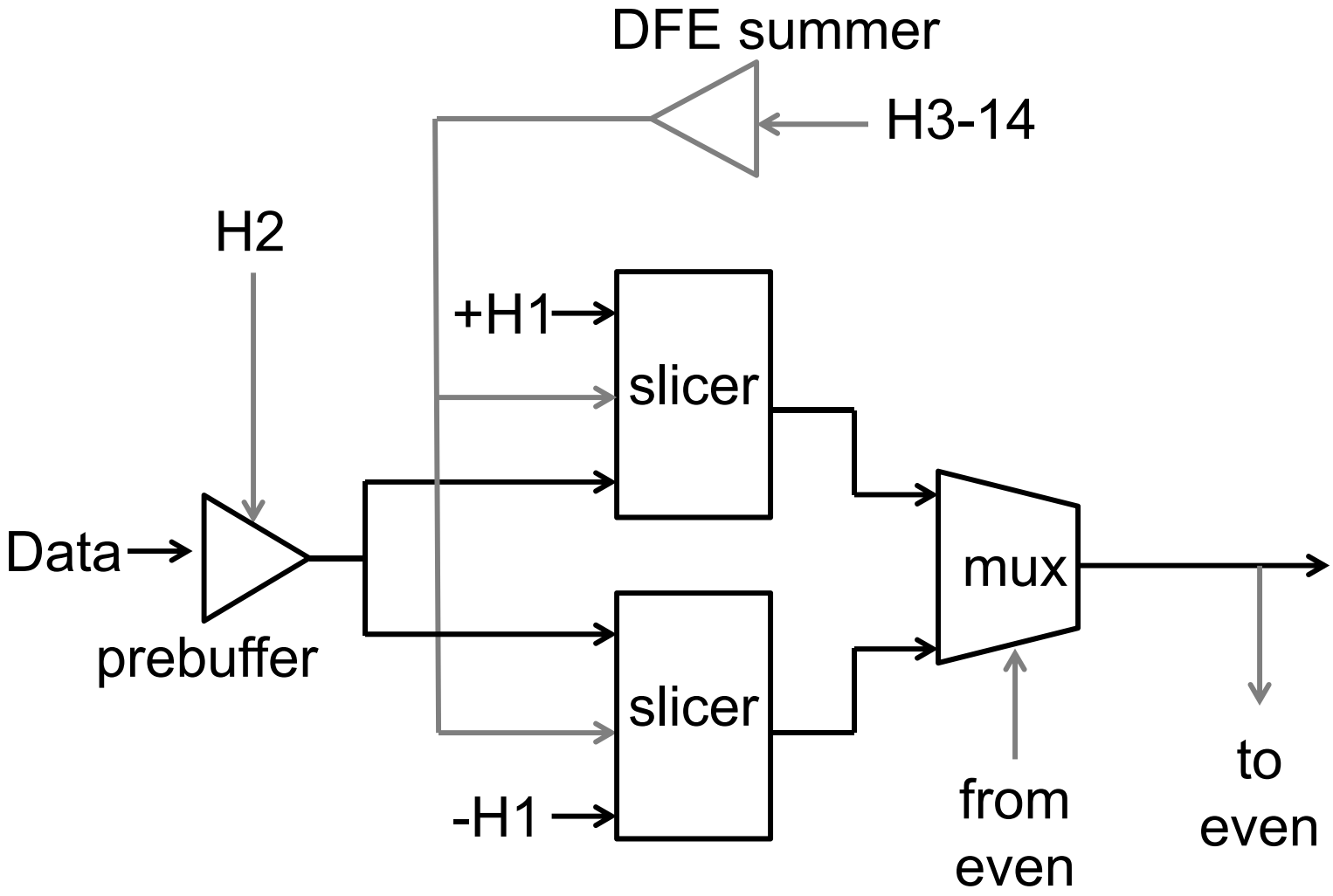
*include AFE + buffer + DFE prebuffer.
also 2~3dB loss from package and PCB trace.

DFE block Diagram

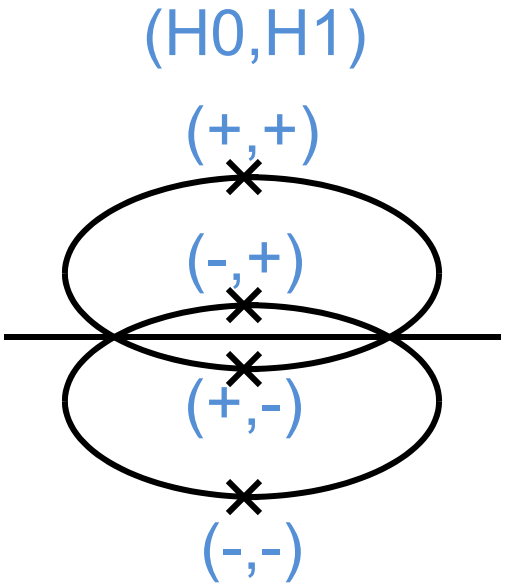
- Half rate design of 14 tap DFE
- Unrolled H1 to relax the critical timing
- Minimum number of error latch



DFE feedback



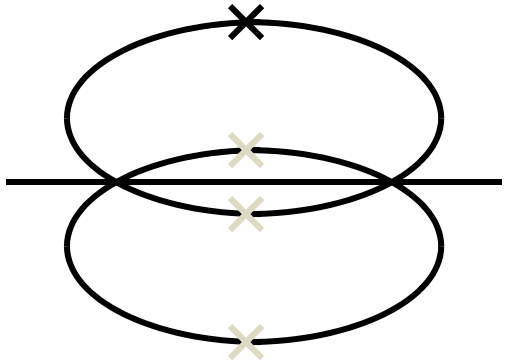
Error position for unrolled DFE



Desire 4 error latches per even/odd slice

⇩

Increase the power and complexity



Use only 1 error latch.

- programmable
- dynamically rotatable

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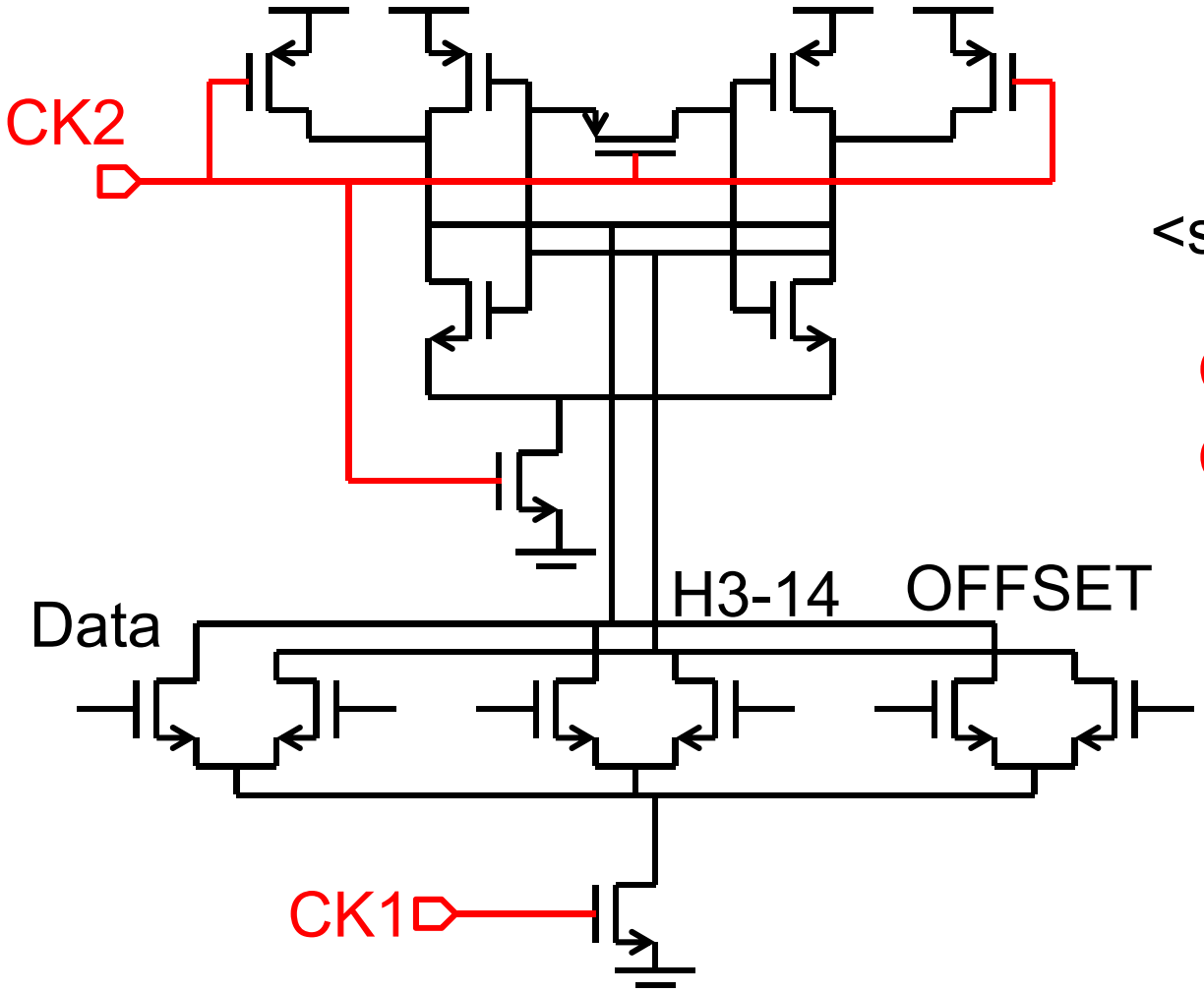
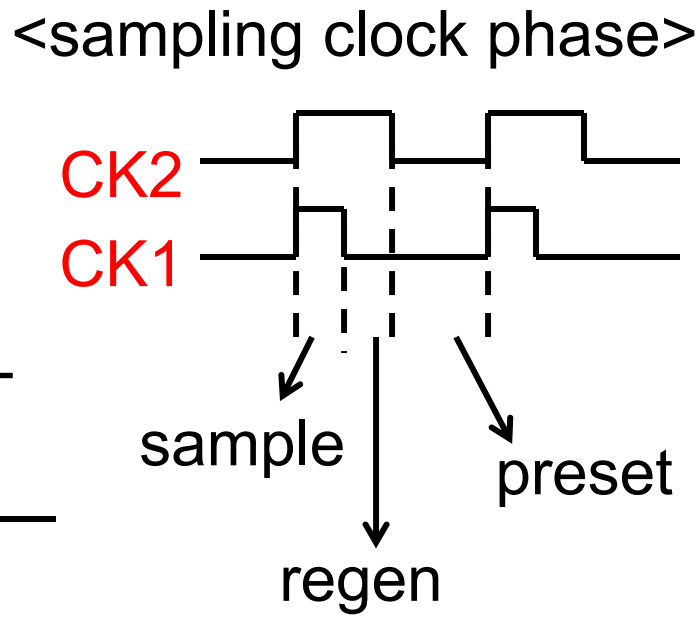
Save power and area without performance loss

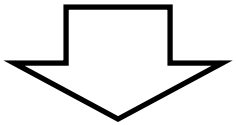
DFE Slicer Circuit Diagram





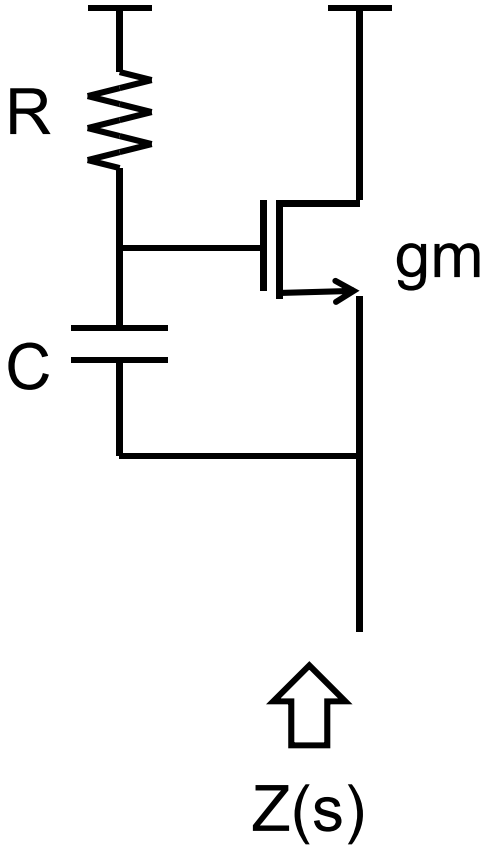
Clock Distribution Scheme

- Many High speed clock buffers are used for clock distribution
- Buffer bandwidth, power, and area are very critical



- Clock buffer with active inductor loading to achieve high BW, low power and small area.

Conventional Active Inductor Load



$$Z(s) = \frac{sCR + 1}{gm}$$

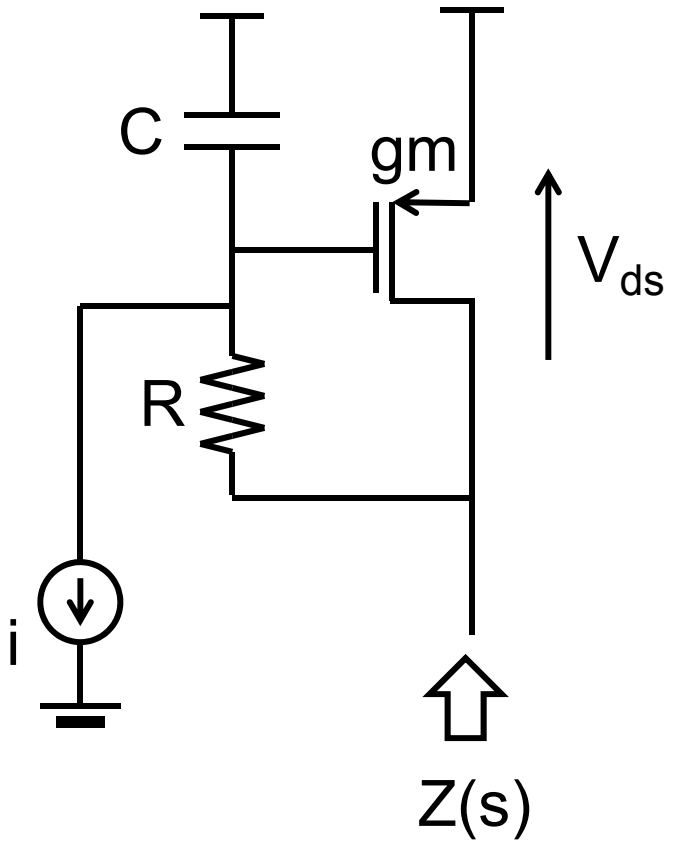
<Advantage>

- Bandwidth improvement by adding zero

<Disadvantage>

- Head room by Vgs.
- Native Device to relax Vgs
  - Large channel length

PMOS Active Inductor Load



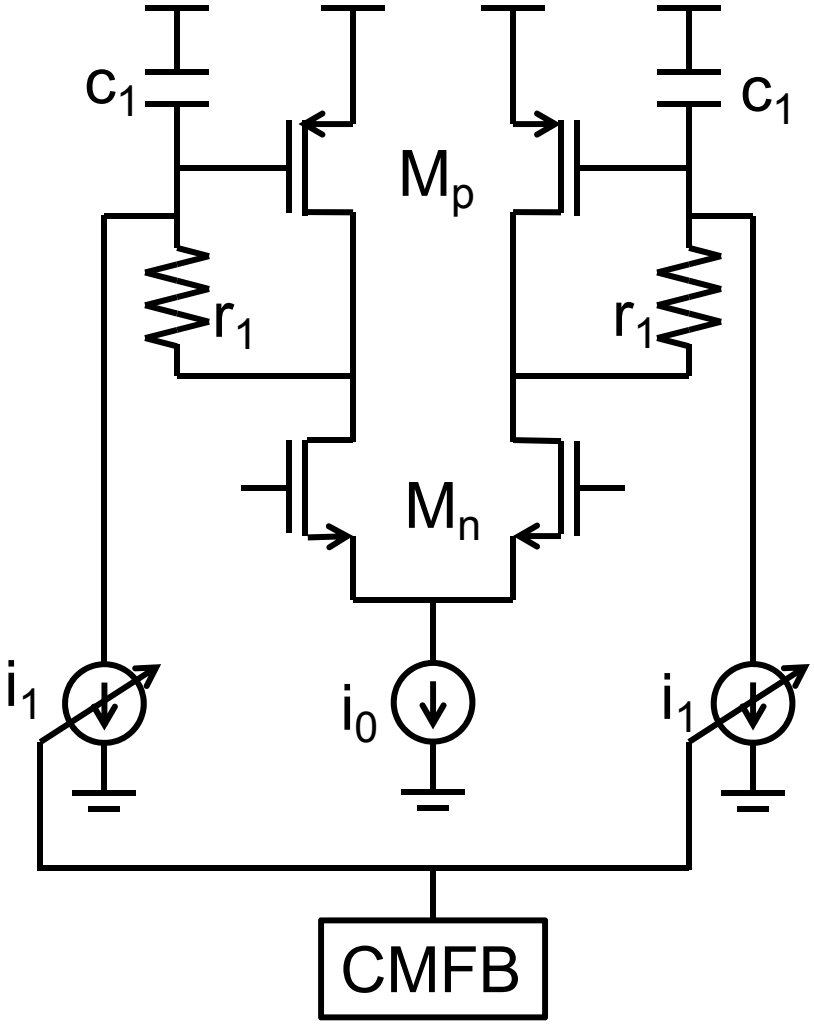
$$V_{ds} = V_{gs} - iR$$

- Head room improve by iR.
- By controlling i, control the common mode voltage.

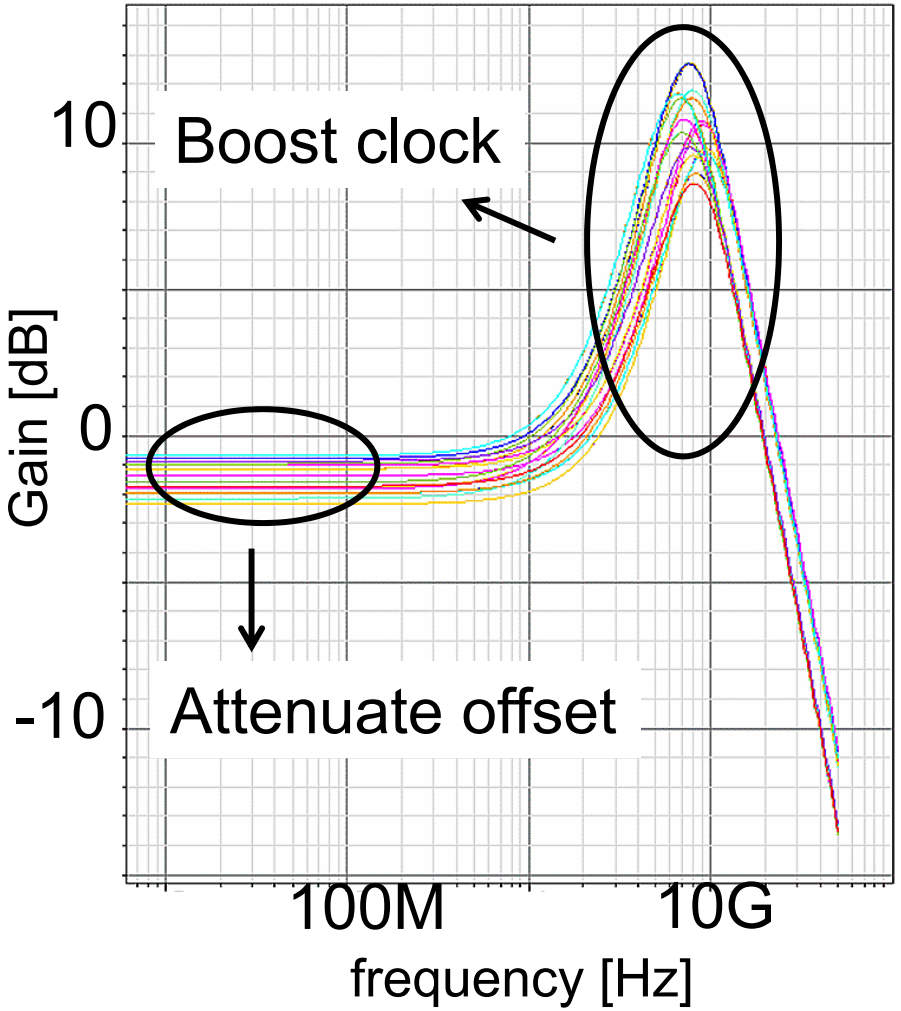
⇩

- CMFB to control the i.

Active Inductor Clock Buffer Circuit

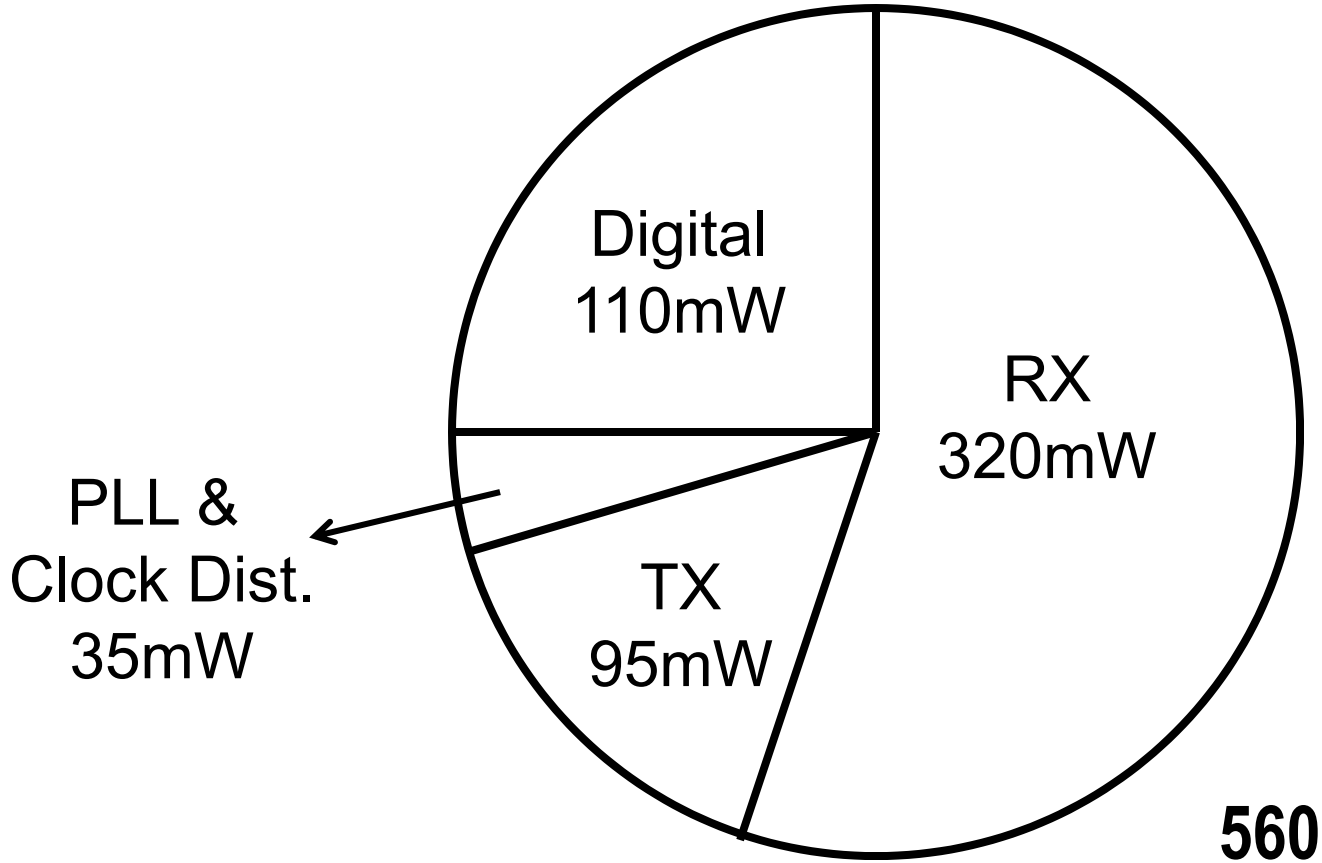


Simulated frequency response



Worst Case Power Breakdown

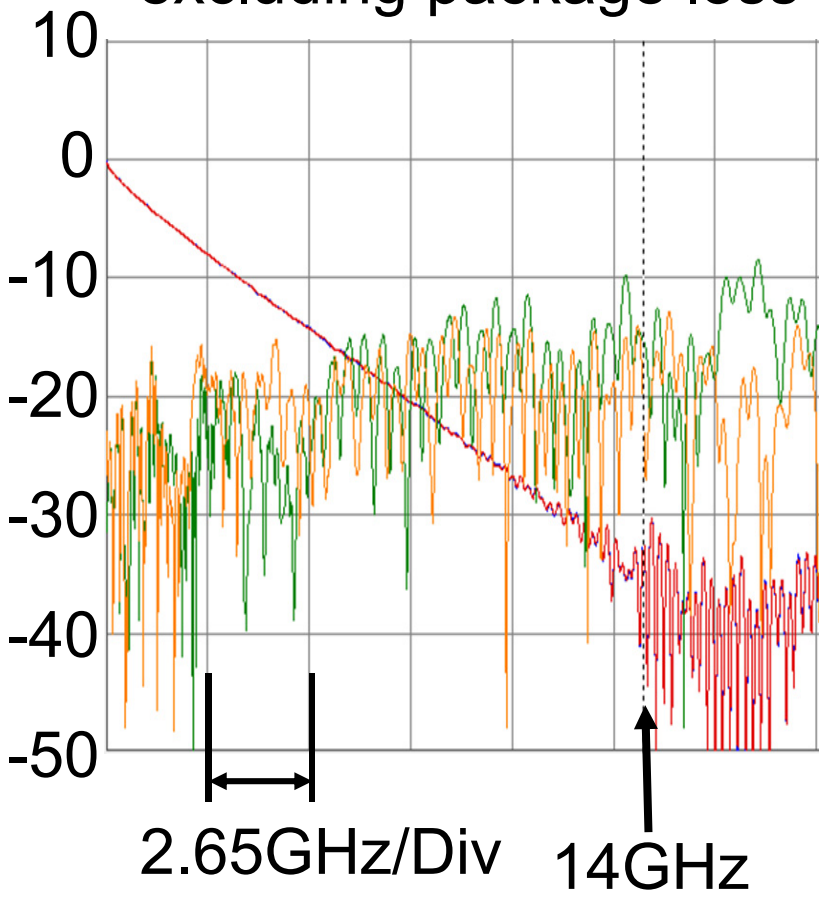
28Gbps 4 lane 1 PLL configuration.



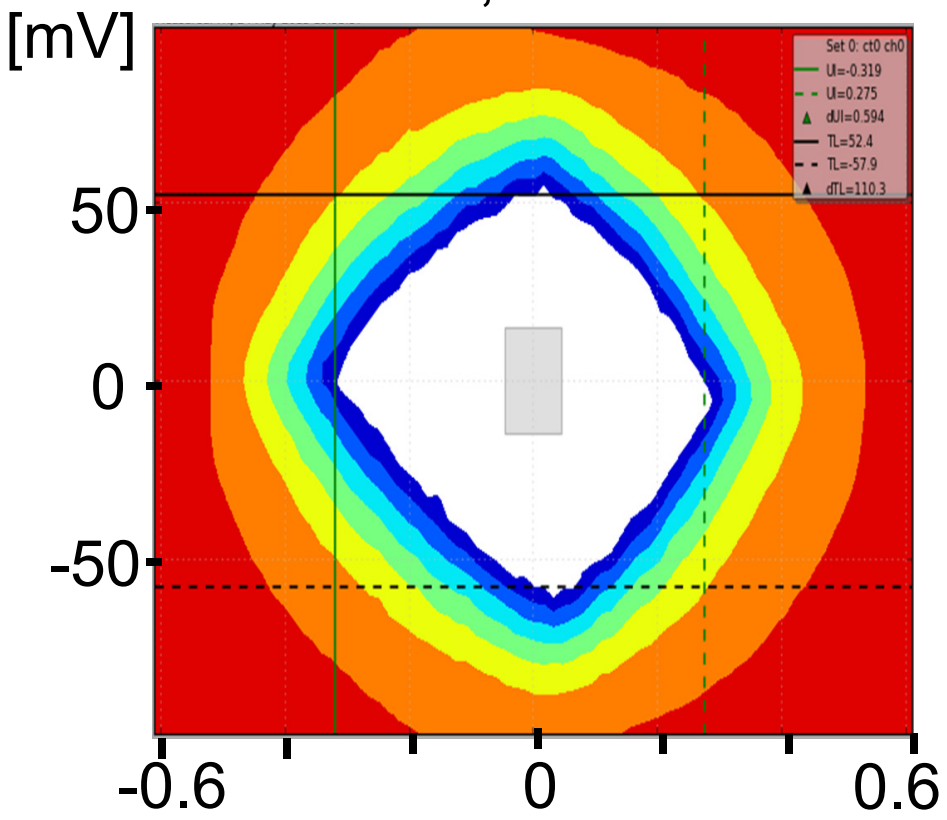
560 mW / lane
(3 sigma ff corner, temp=125)

Measured Eye Diagram at 28Gbps

Measured test channel
Total IL = 34dB
excluding package loss



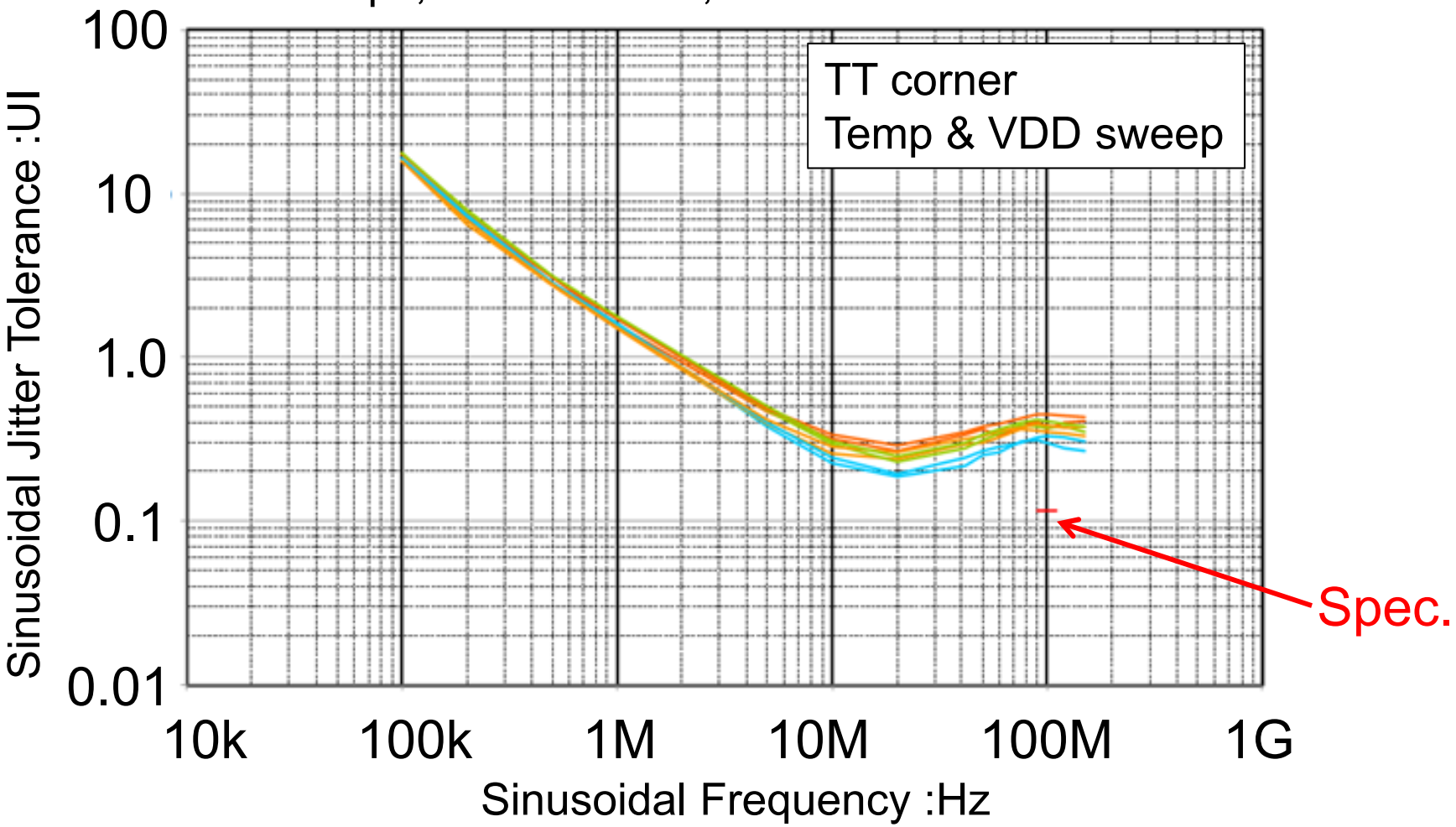
Eye margin @ 10E-9
HM=0.6UI, VM=110mV



HM: Horizontal margin
VM: Vertical margin

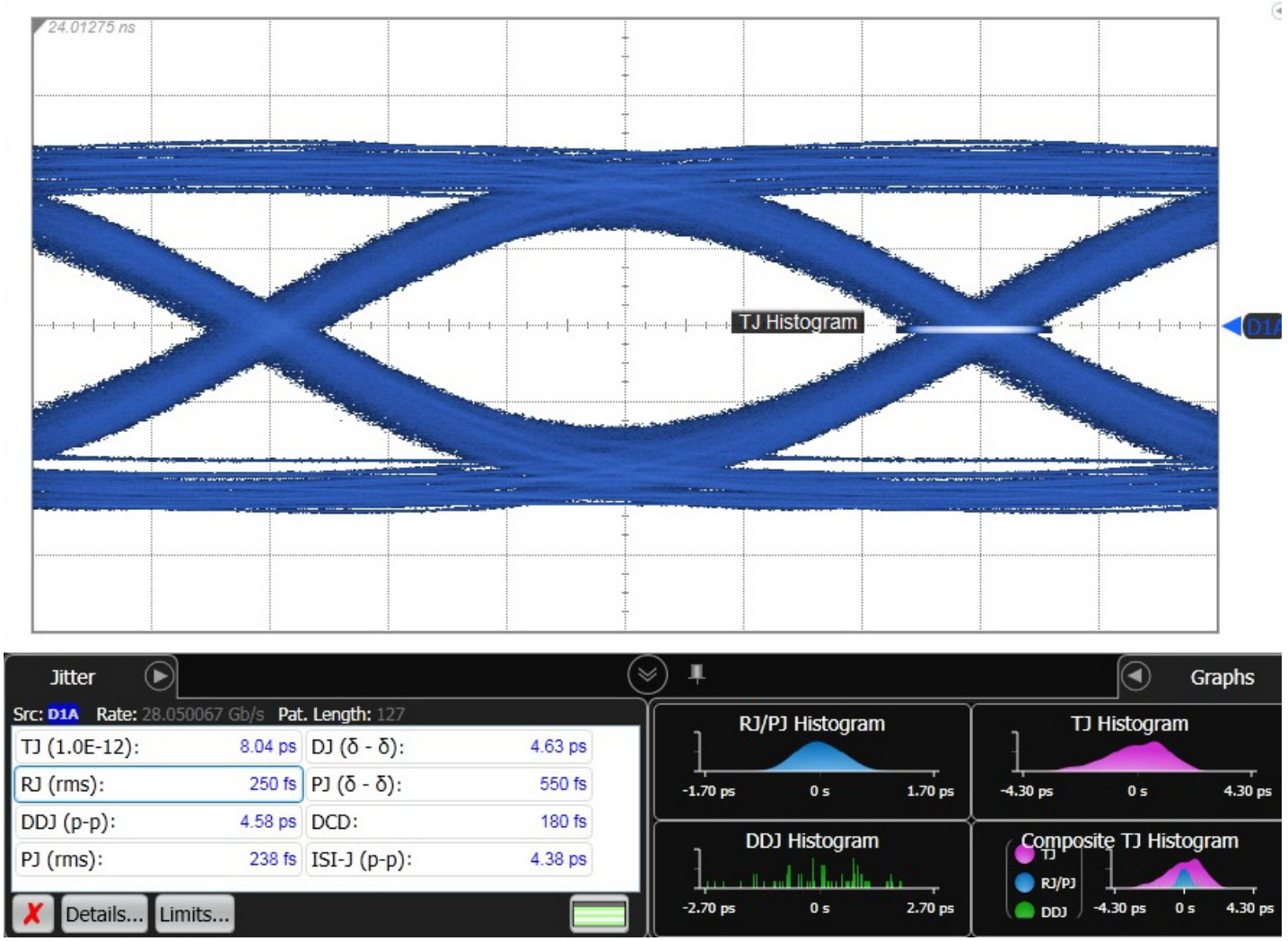
100G-KR SJ tolerance measurements

Test channel: 31.5dB loss @ 12.9GHz
Include all other impairments (cross talk & random interference)
25.8Gbps, BER=10E-12, PRBS31

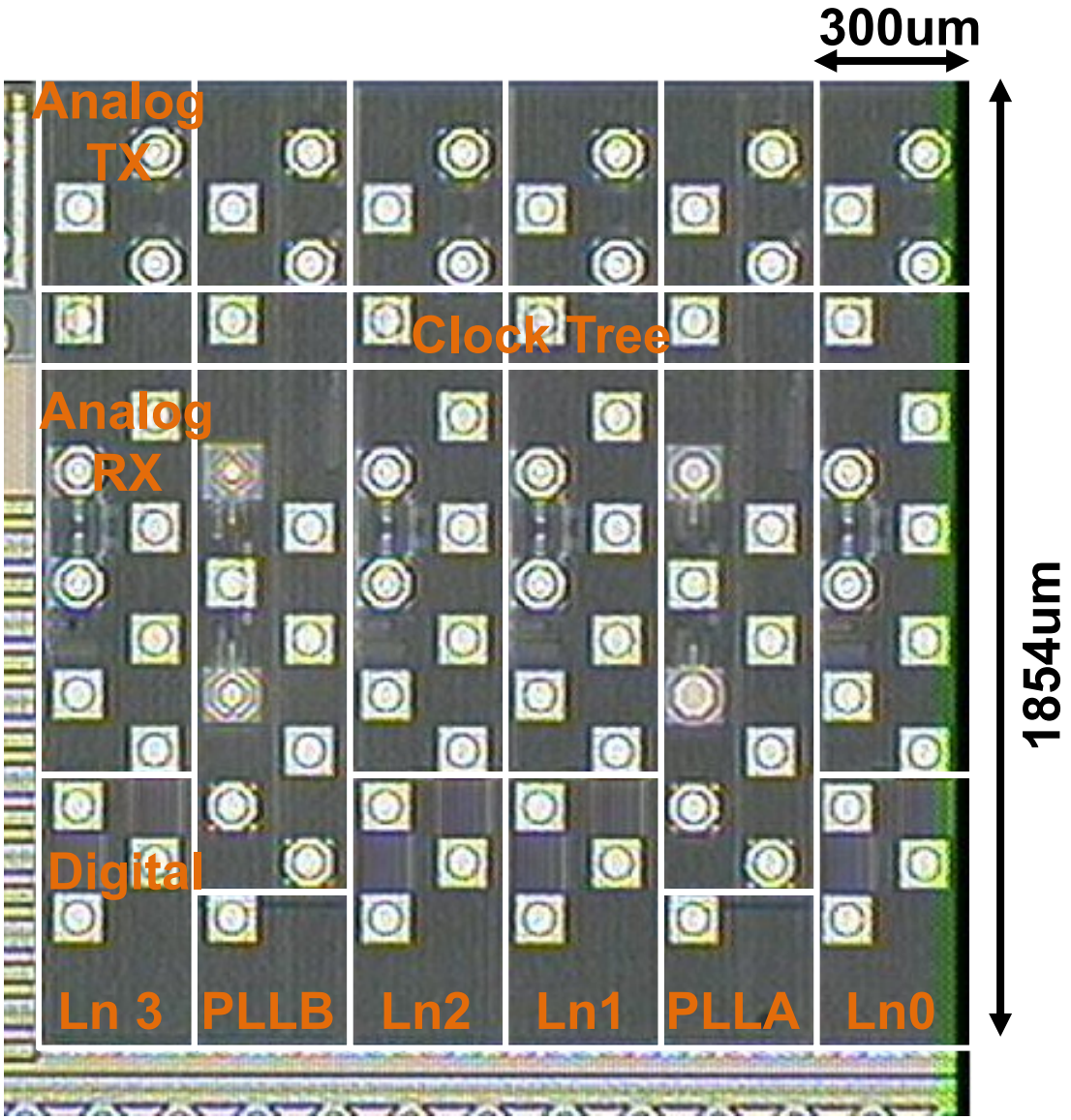


Measured TX output

TX eye diagram of 28G PRBS7 : RJ=250fs, TJ=8ps



Chip Microphotograph



Transceiver Summary

Technology	TSMC 28nm CMOS
Power Supply	1.5V / 1.05V / 0.85V
Area (4 channel+2 pll)	3.34 mm^2
Data Rate Range	1.25 ~ 28.5 Gbps
Channel Loss	34dB @ 14GHz
TX output RJ	250fs @ 28Gbps
Measured Worst Power Consumption	560 mW / lane (3 sigma ff corner, temp=125)

Conclusions

- TIA based AFE achieves 15dB high frequency boost with single pair of inductors
- Half-rate unrolled DFE with 2 rotatable error latches achieves DFE timing closure, less hardware, and robust adaptation
- Group delay algorithm for AEQ adaptation eliminates potential coupling between AEQ and DFE adaptation
- Active inductor clock buffer circuit with CMFB extends bandwidth without major power penalty
- The transceiver achieves error free operation at 28Gbps with 34dB channel loss with worst power of 560mW/lane, and fully complies with multi-standards and applications

A 780mW 4×28Gb/s Transceiver for 100GbE Gearbox PHY in 40nm CMOS

Ullas Singh, Adesh Garg, Bharath Raghavan, Nick Huang,
Heng Zhang , Zhi Huang, Afshin Momtaz, Jun Cao

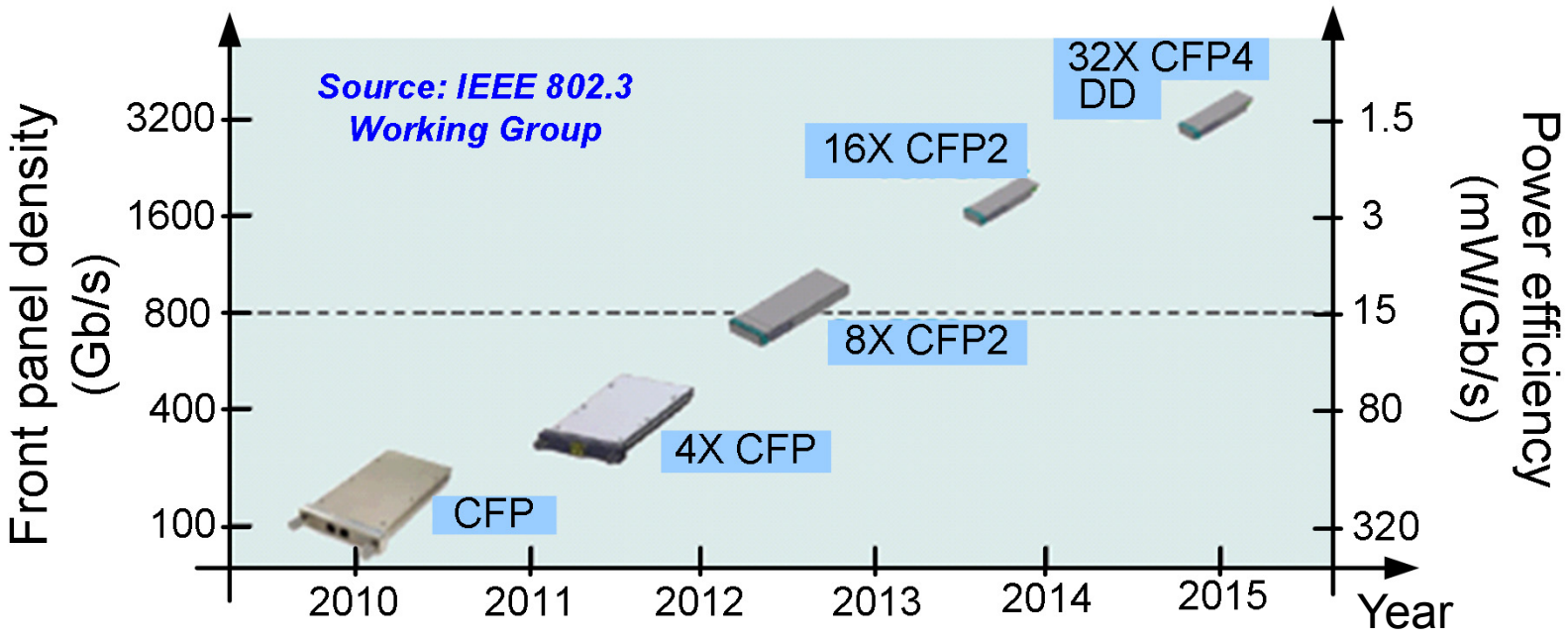
Broadcom, Irvine, CA

Outline

- Motivation
- Transmitter
- Receiver
- PLL and Clock Distribution
- Measurement Results
- Comparison and Summary

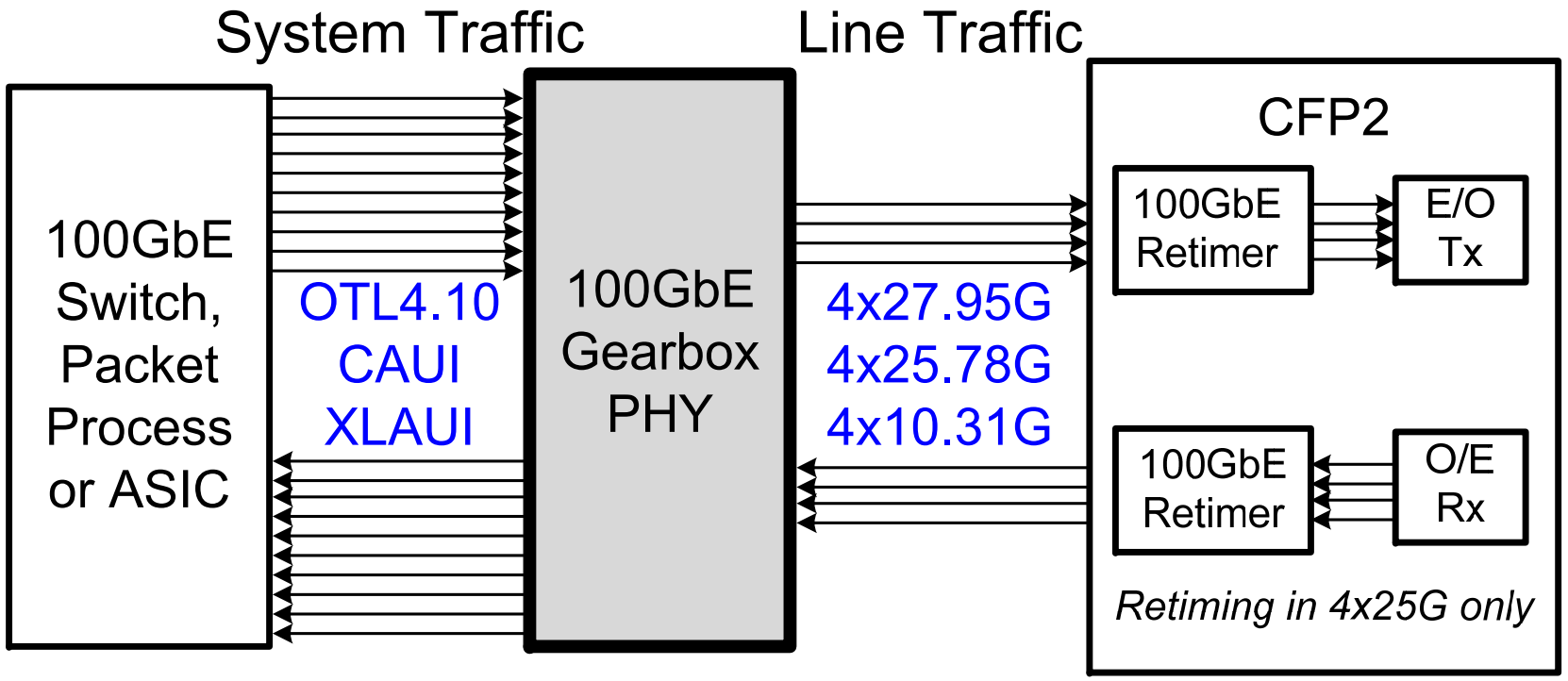
Motivation

- Trends in 100Gb/s Optical Ethernet
  - Bandwidth demand is growing and driving panel density
  - Power of optical module is being reduced



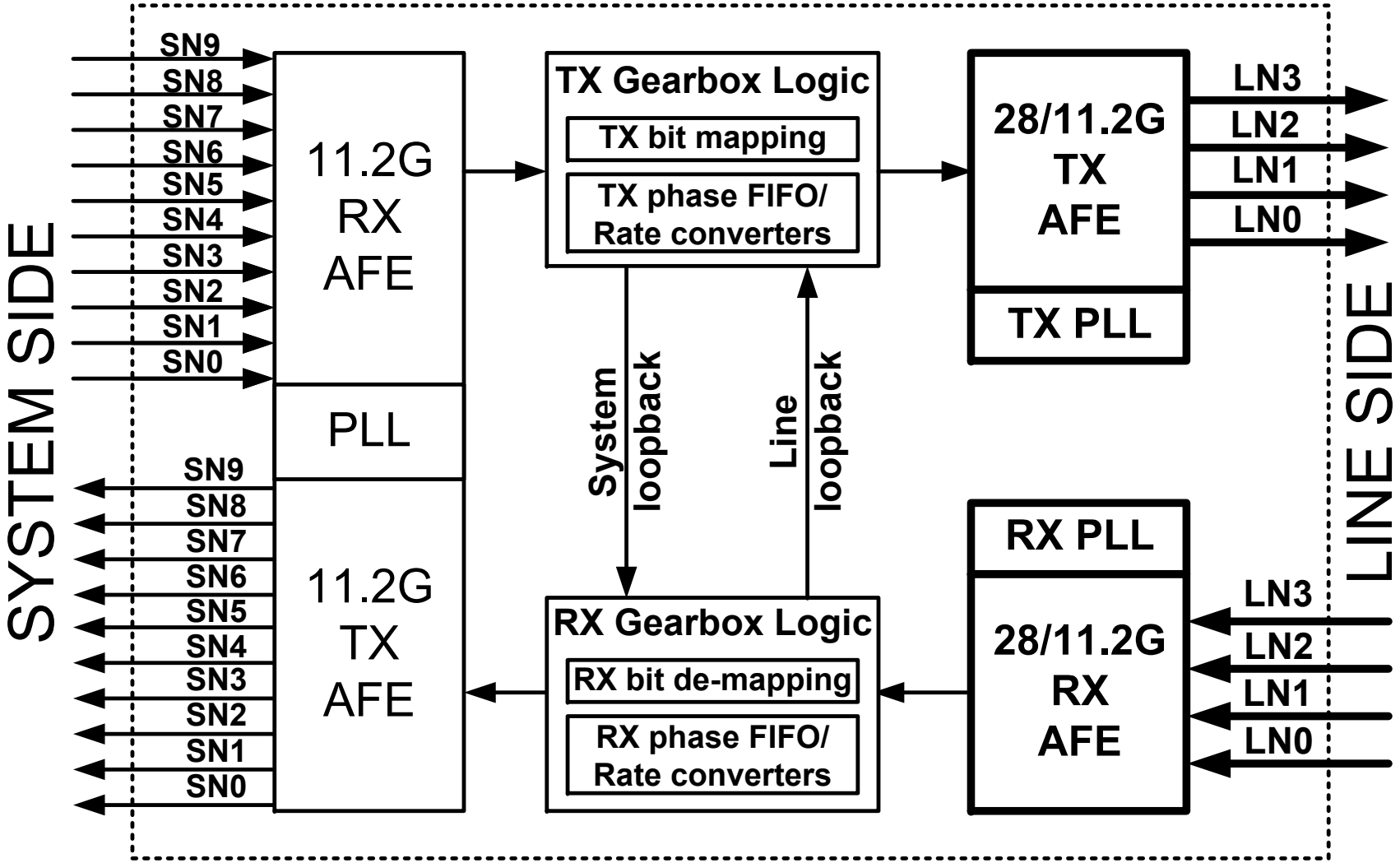
Motivation

- Gearbox PHY power needs to scale with optical module power
- Gearbox PHY needs to support multiple operational modes



Need a low-power, reconfigurable gearbox transceiver

100GbE Gearbox PHY Chip



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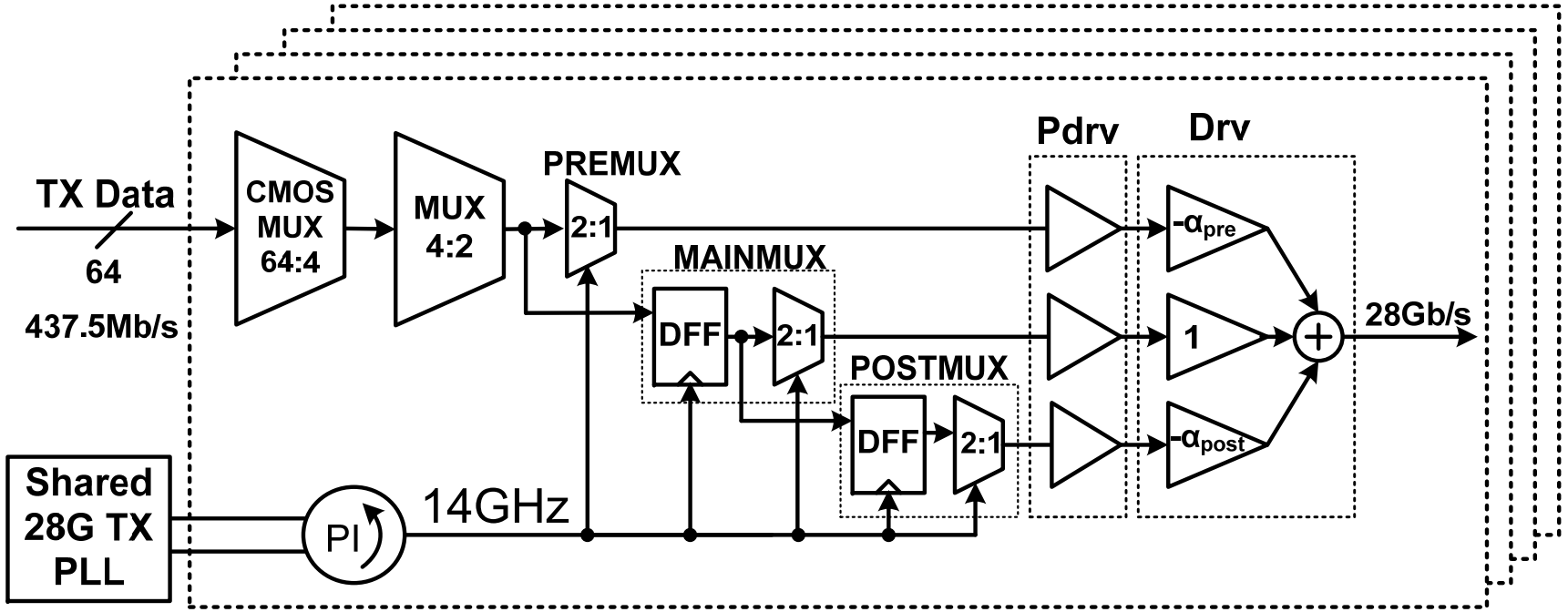
28Gb/s Transmitter

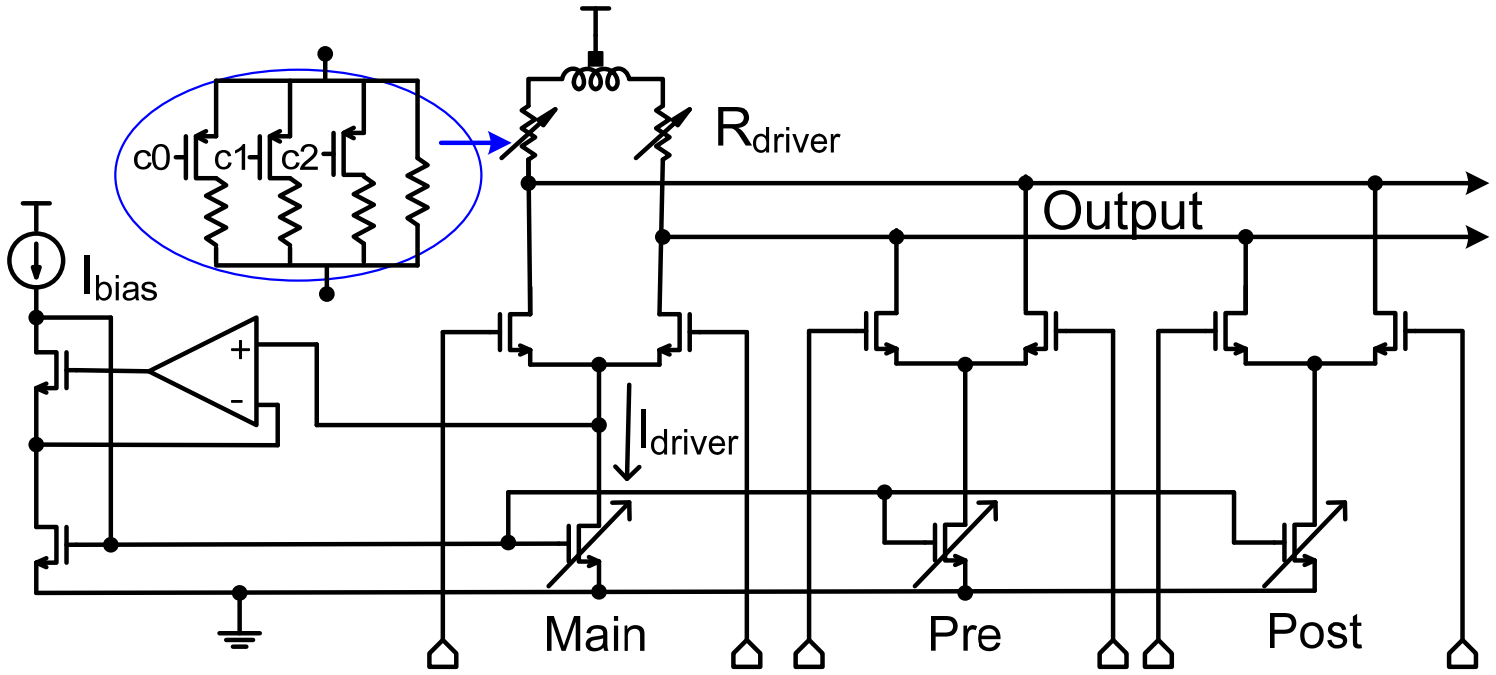


- Half-rate operation with a 14 GHz TX clock
- Phase interpolator (*PI*) for independent phase adjustments

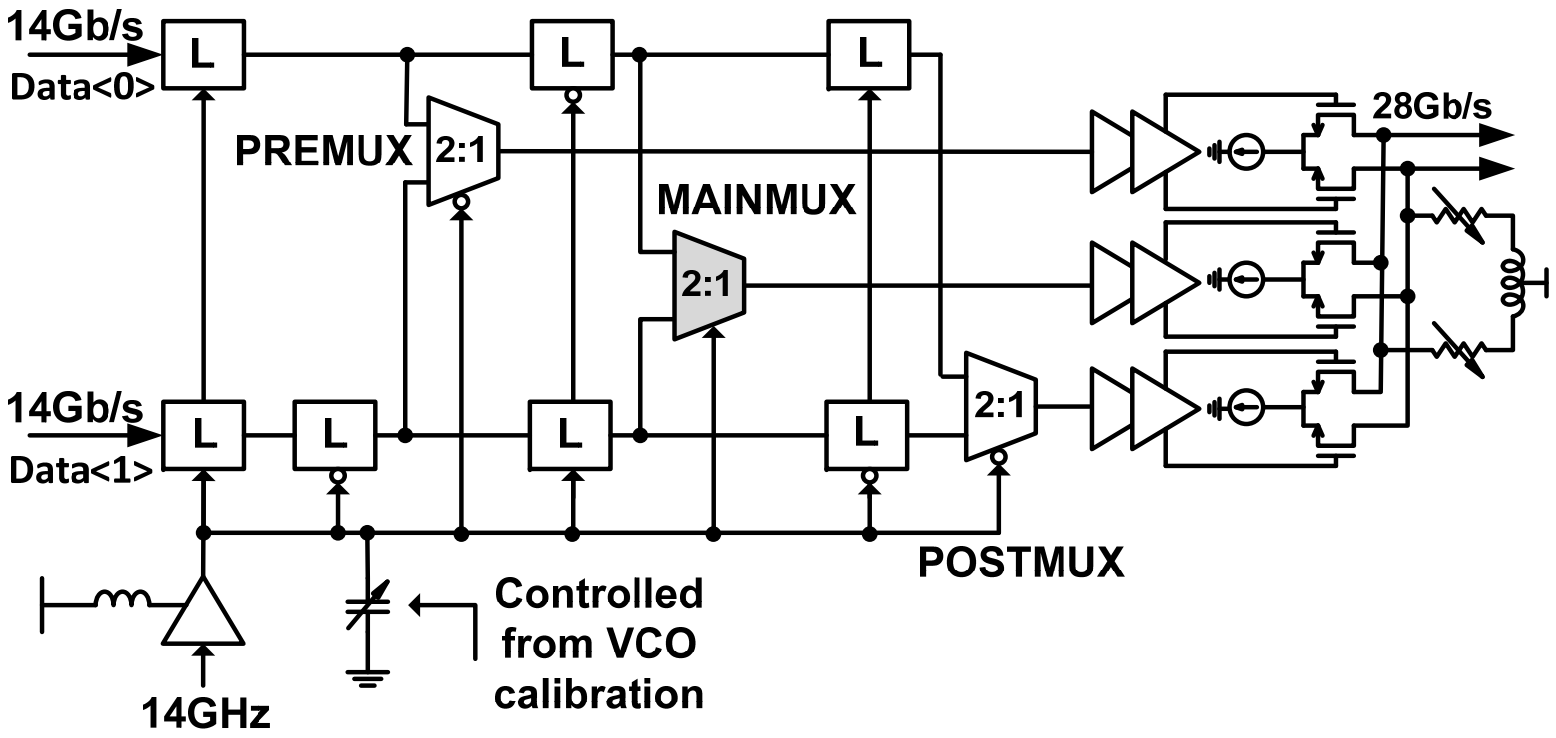
28Gb/s Driver Circuit

- Swing variation is reduced to decrease the driver size
  - R_{driver} is digitally calibrated
  - I_{driver} variation is reduced using feedback loop.

⇒ Overall Swing Variation is only ±5% across PVT



2:1 CML MUX AND CLOCK



- Main Path is optimized to improve power/performance
  - Inductive peaking for lower power
  - Clock-Up Mux for lower ISI [*B Raghavan, et al., ISSCC 2013*]
- Single-tuned clock driver for a large clock load

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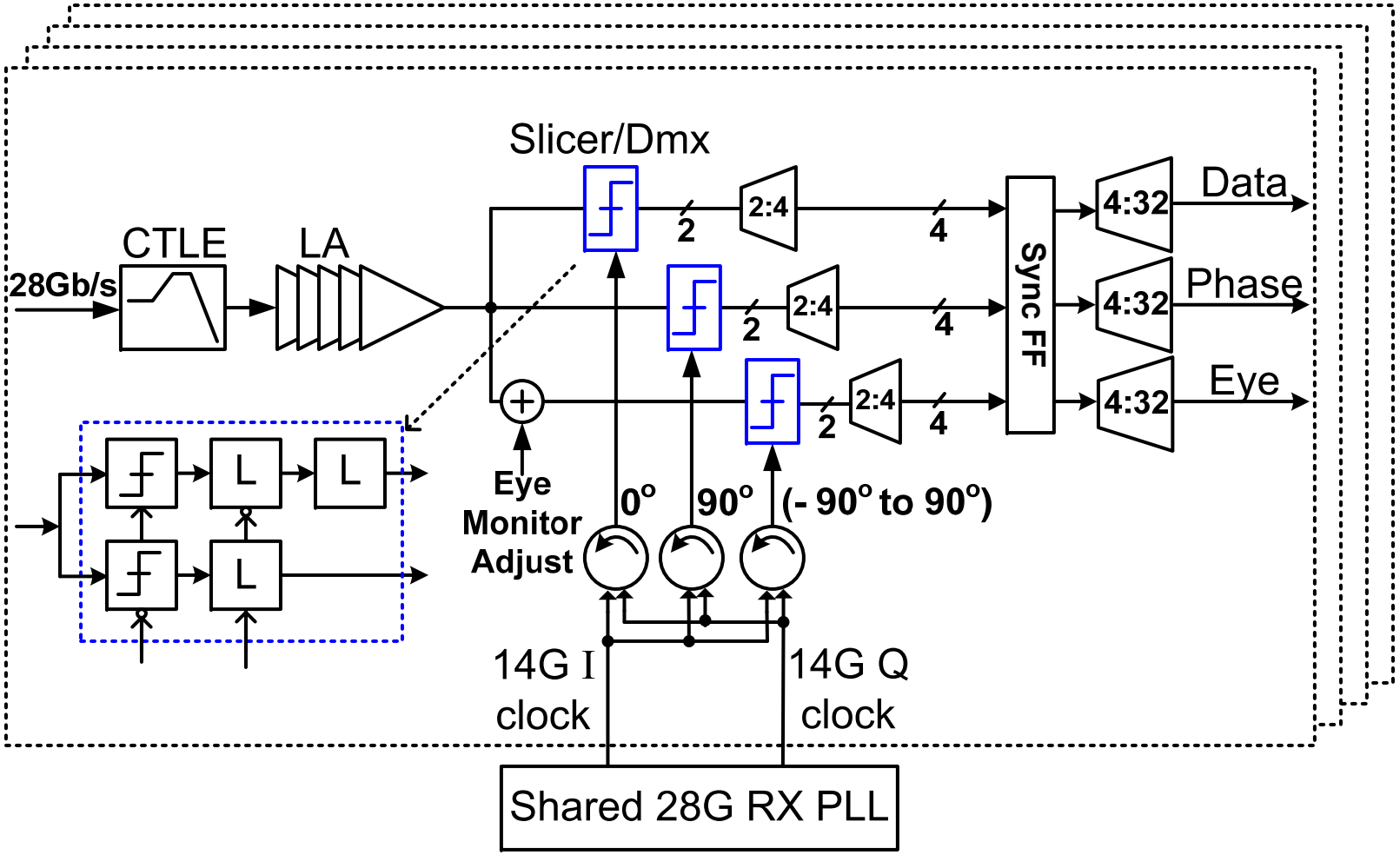
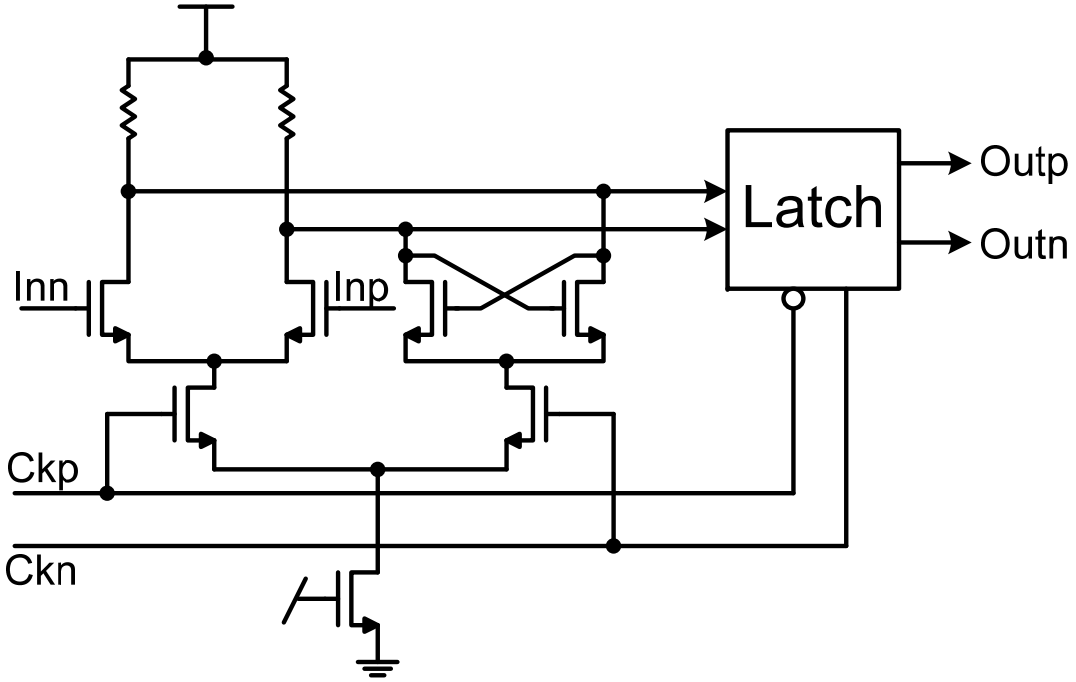
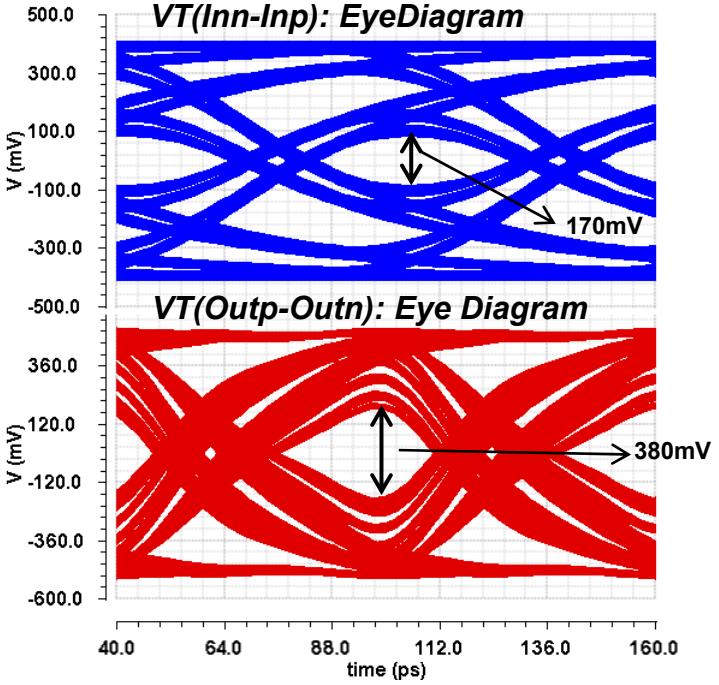
Receiver Architecture



- Half-rate operation with a 14 GHz RX Clock

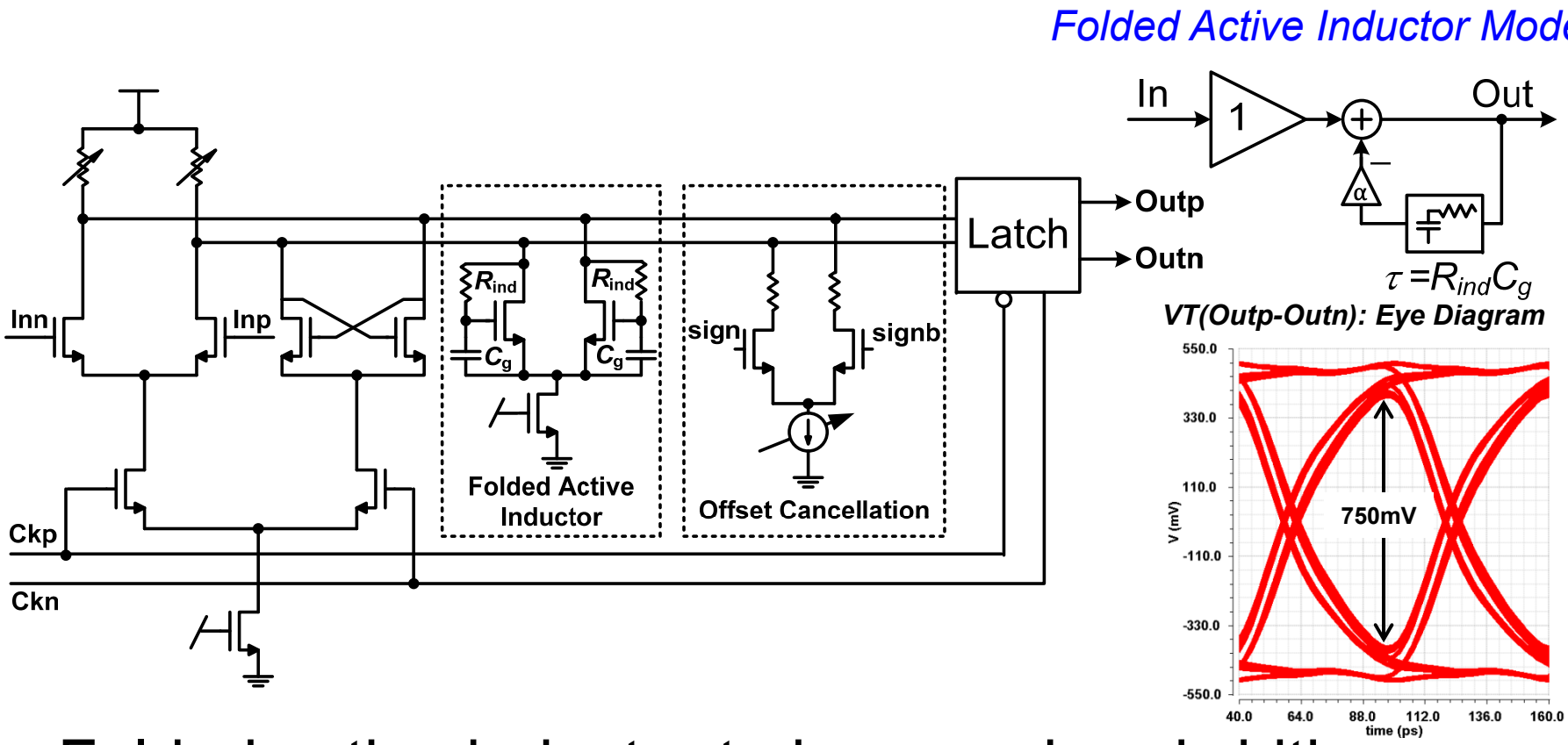
Conventional High-Speed Slicer





- CML latch-based slicer is used for BW enhancement
  - Higher bandwidth for improved sensitivity (Power ↑)
  - Reduced slicer size to reduce loading to the LA (Offset ↑)

Proposed High-Speed Slicer



- Folded active inductor to improve bandwidth
  - Transfer Function: $H(s) = \frac{1}{1+\alpha}\left(\frac{1+s\tau}{1+s\tau/(1+\alpha)}\right)$; $\tau = R_{ind}C_g$
- Slicer offset is calibrated using the current DAC

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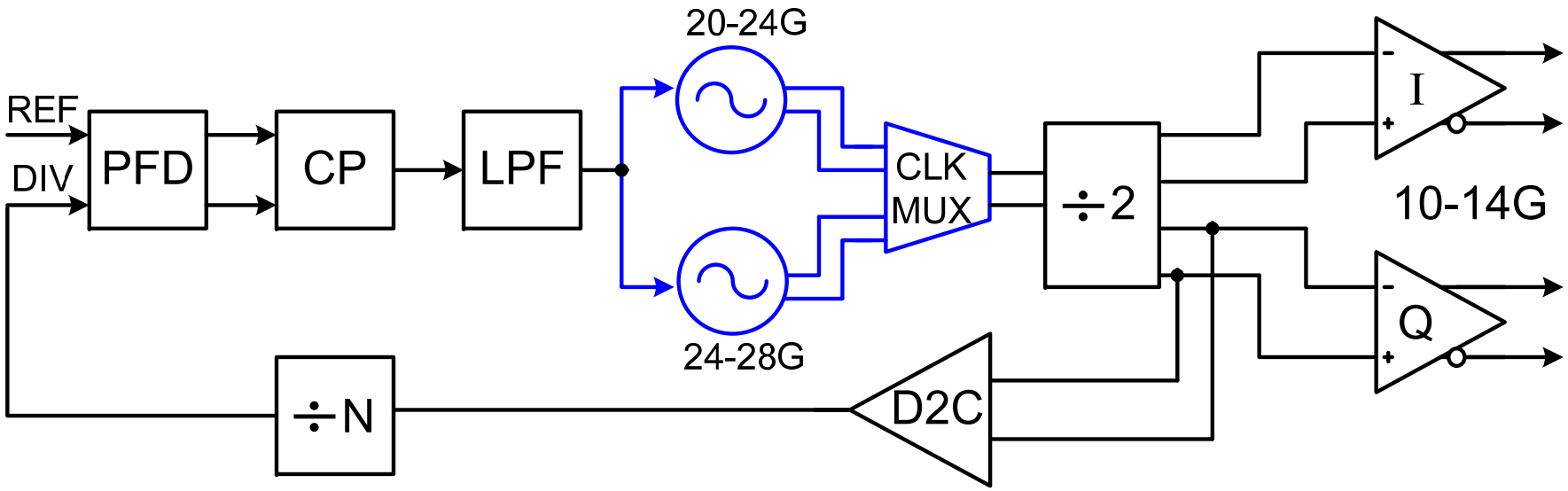
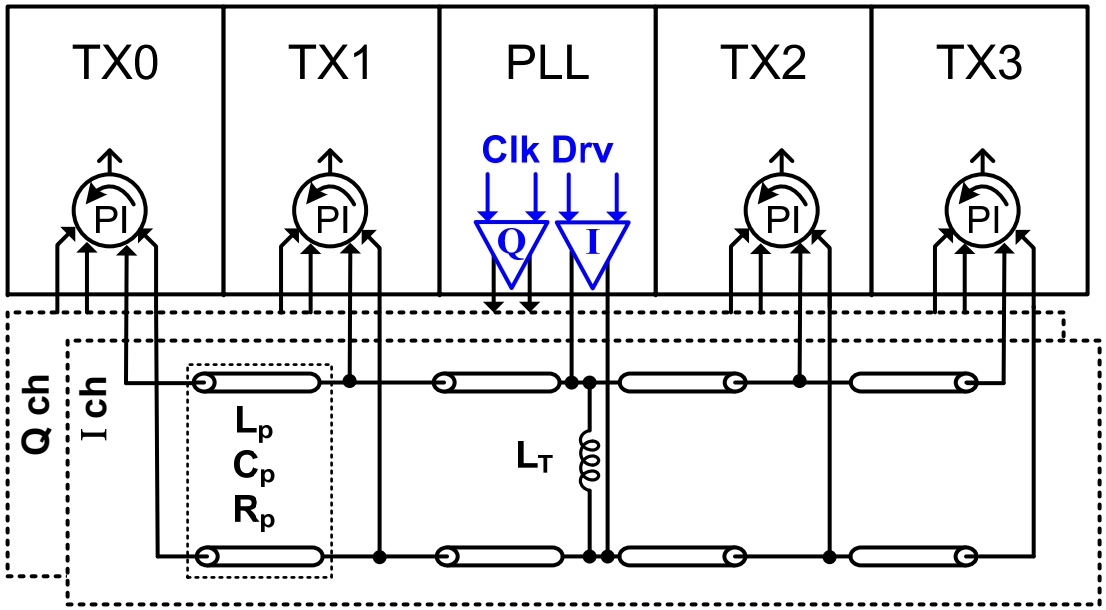
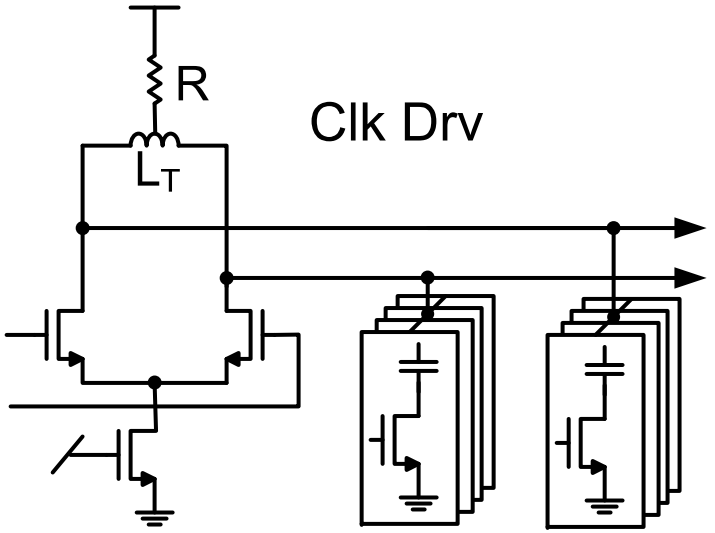
PLL Schematic



- Very wide operating range (20G-28G)
  - Dual LC VCO architecture
- Output of VCO is selected using a low-Q tuned MUX

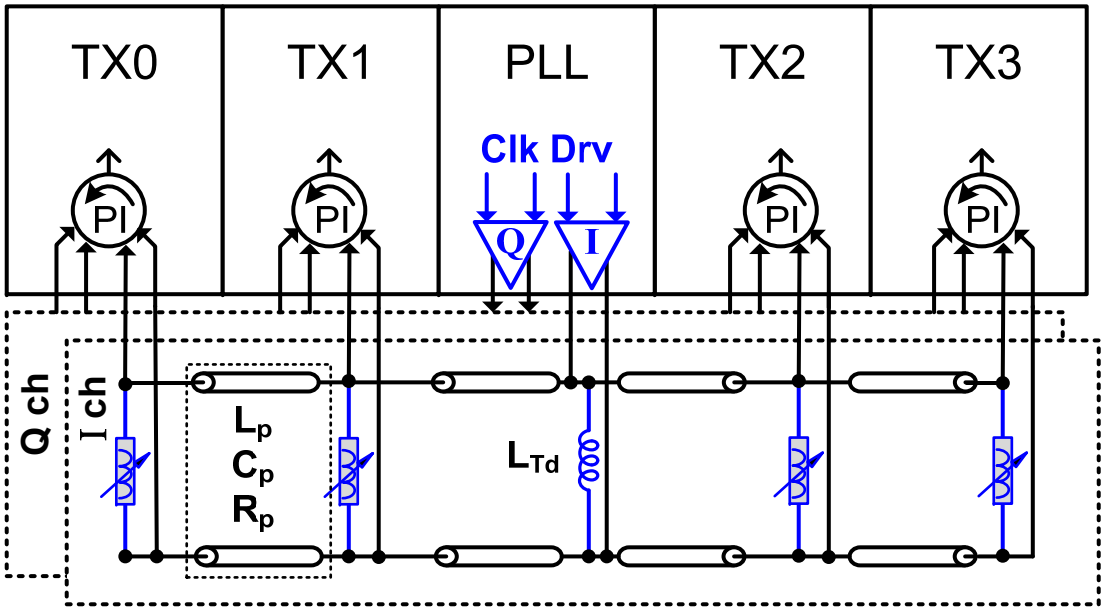
Conventional Clock Distribution

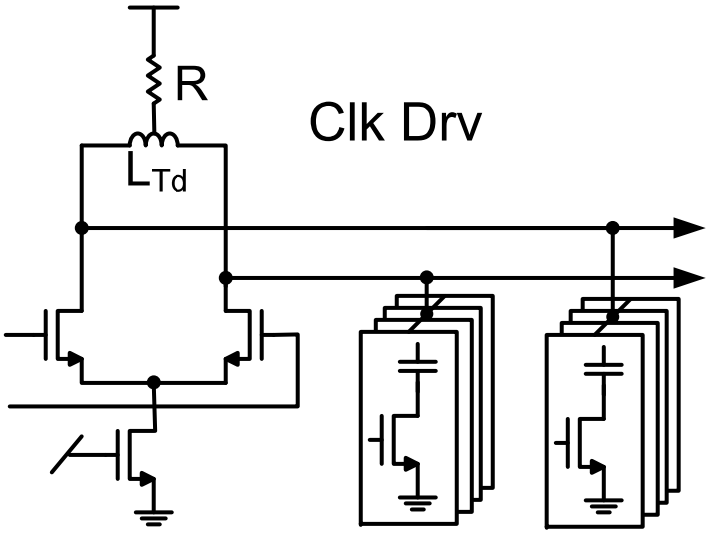




- Source-tuned circuit to operate from 10-14 GHz
  - Resonant frequency and clock amplitude depends on parasitic inductor (L_p)
- Capacitance bank to tune the frequency of the operation
  - Amplitude depends on operating frequency ($V_{amp} \propto \omega L$)

Proposed Clock Distribution

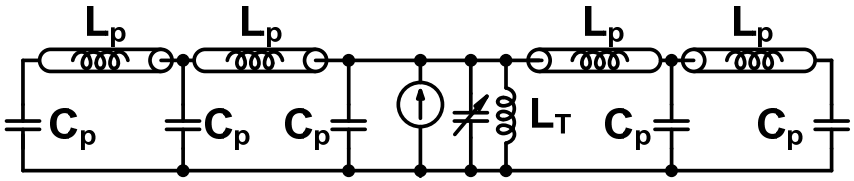


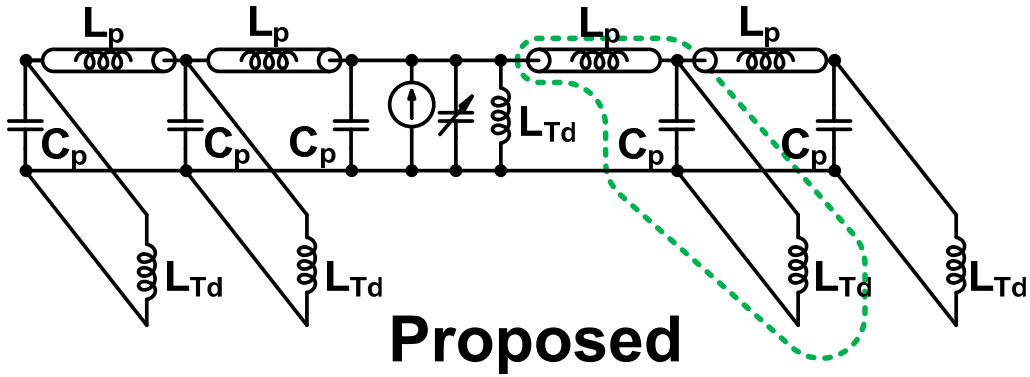


- Distribute the inductor along the interconnect to create local resonance
  - Resonant frequency and clock amplitude independent of L_p
- Switched inductor to tune the frequency of operation

Clock Distribution Comparison

- Interconnect model with driver





Conventional

$$f_{src} \sim \frac{1}{\sqrt{5L_T C_P \left(1 + \frac{3L_P}{5L_T}\right)}}$$

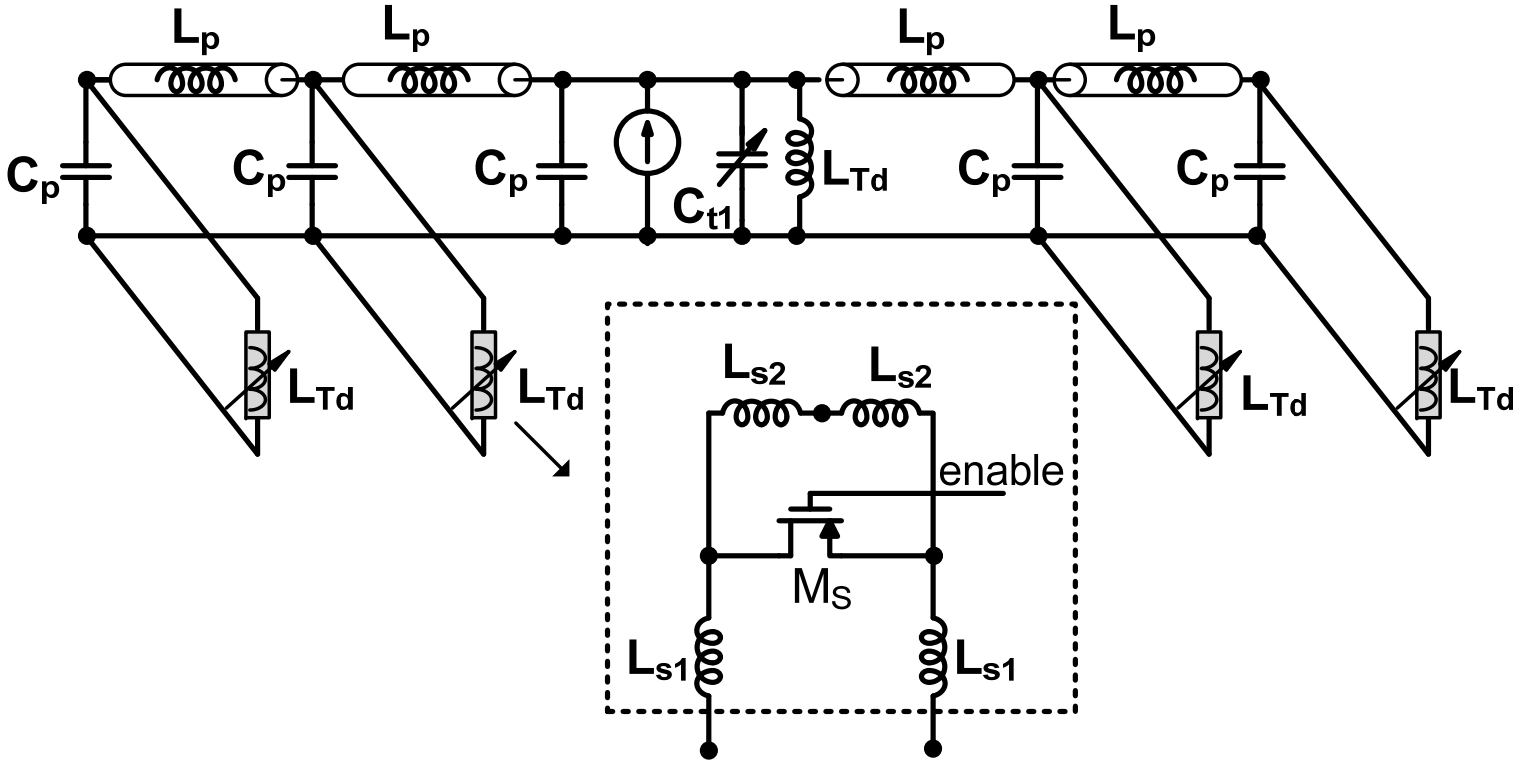
- f_{src} **dependent** on L_p
- Lower amplitude ($\propto \omega L_T$)

Proposed

$$f_{srp} \sim \frac{1}{\sqrt{L_{Td} C_P}}; \; L_{Td} \sim 5L_T$$

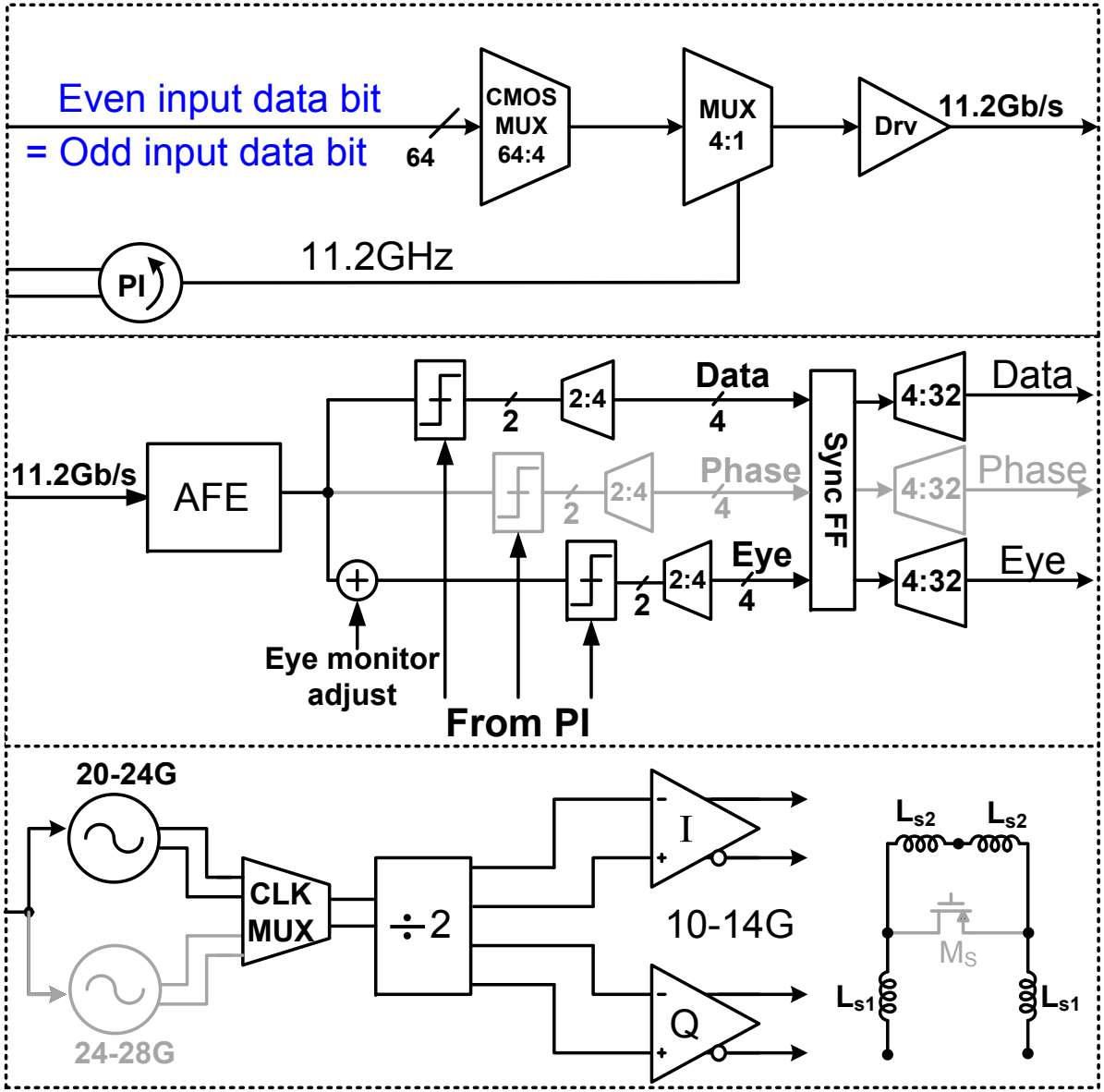
- f_{srp} **independent** of L_p
- Higher amplitude ($\propto \omega L_{Td}$)

Frequency Tuning of Clock Distribution



- Switched inductor to tune the frequency
  - f_{so}=12-14G; switch (M_s) is closed ($L_{Td}=2L_{s1}$)
  - f_{so}=10-12G; switch is open, $L_{Td}=2(L_{s1}+L_{s2})$

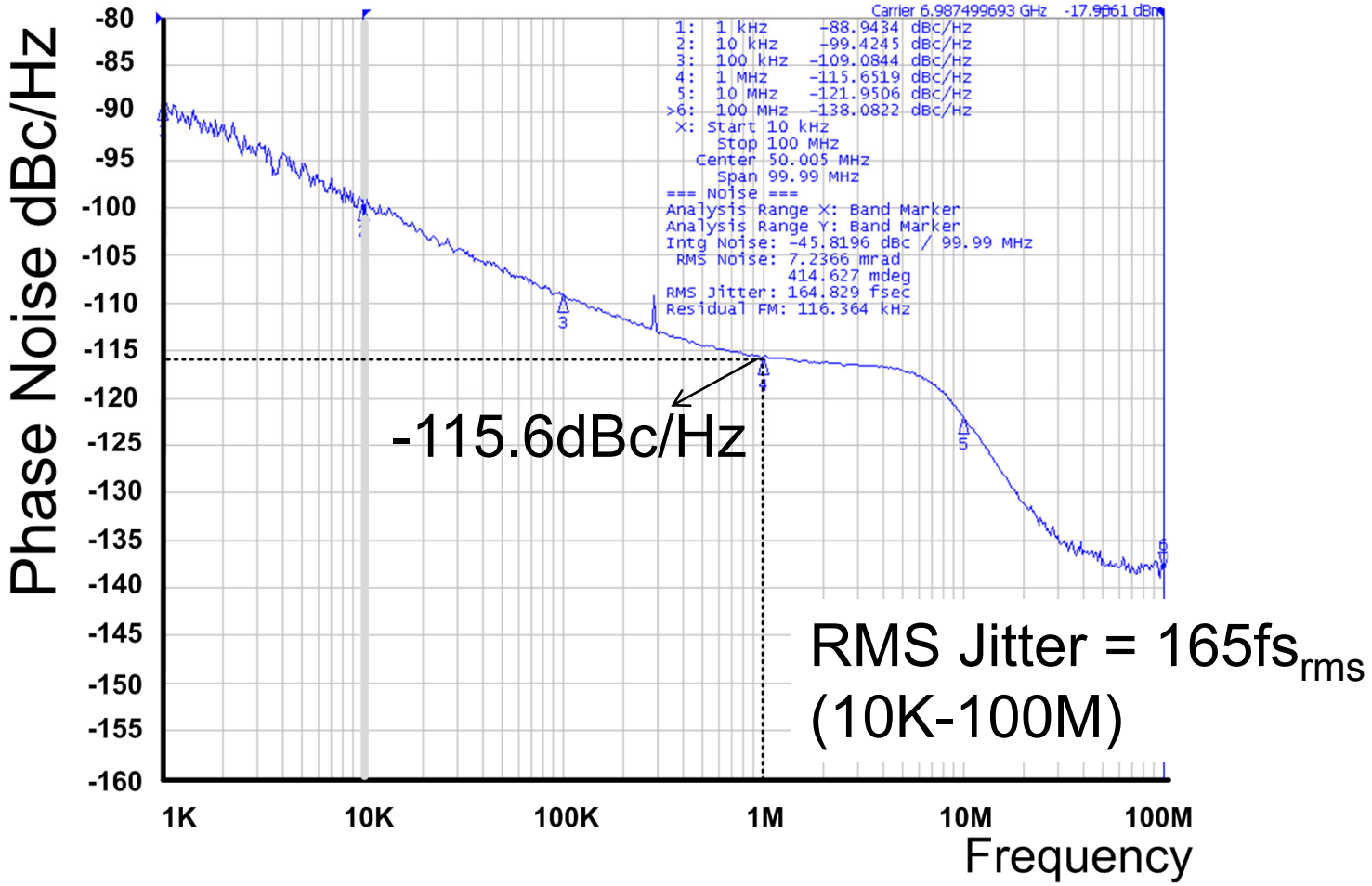
Reconfiguration for 4×11.2Gb/s Operation



Outline

- Motivation
- Transmitter
- Receiver
- PLL and Clock Distribution
- **Measurement Results**
- Comparison and Summary

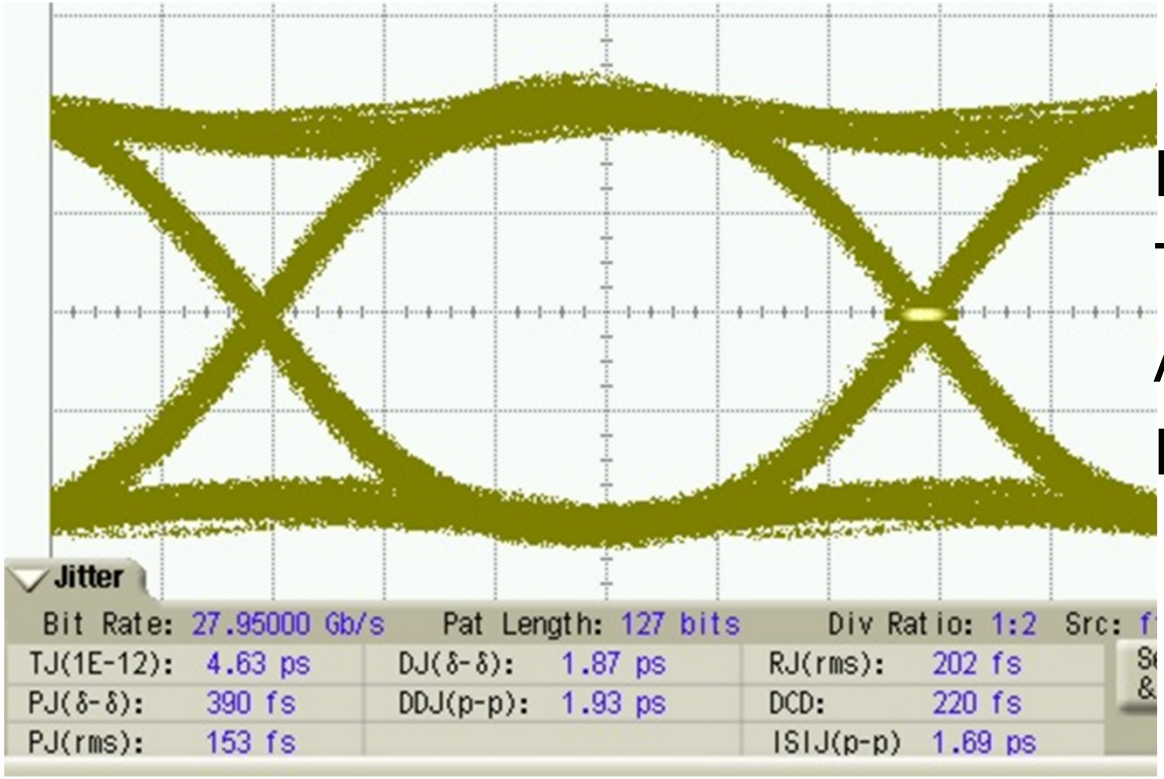
Measured PLL Clock Spectrum



- Phase noise measurement using divide-by-4 clock (7G)
- Calculated 27.9G clock, PN= -103.5dBc/Hz @1MHz

Measured Transmitter Eye Diagram

- The chip is packaged in a standard plastic BGA
- Data rate: 27.95Gb/s



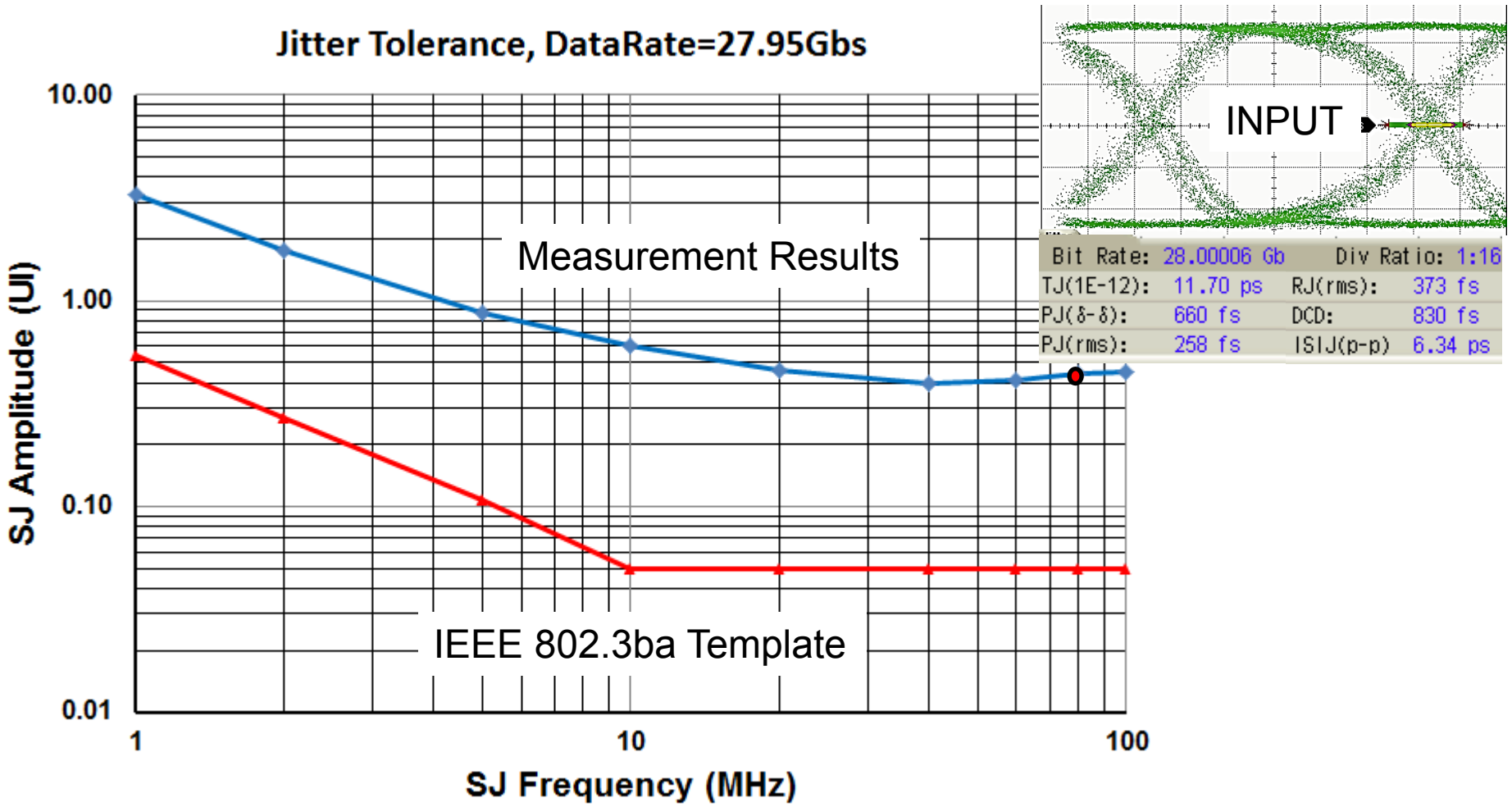
DJ_{pp} : 1.87ps

TJ_{pp} (BER=10^{-12}) : 4.6ps

Amp: 600 $mV_{pp\text{-}diff}$

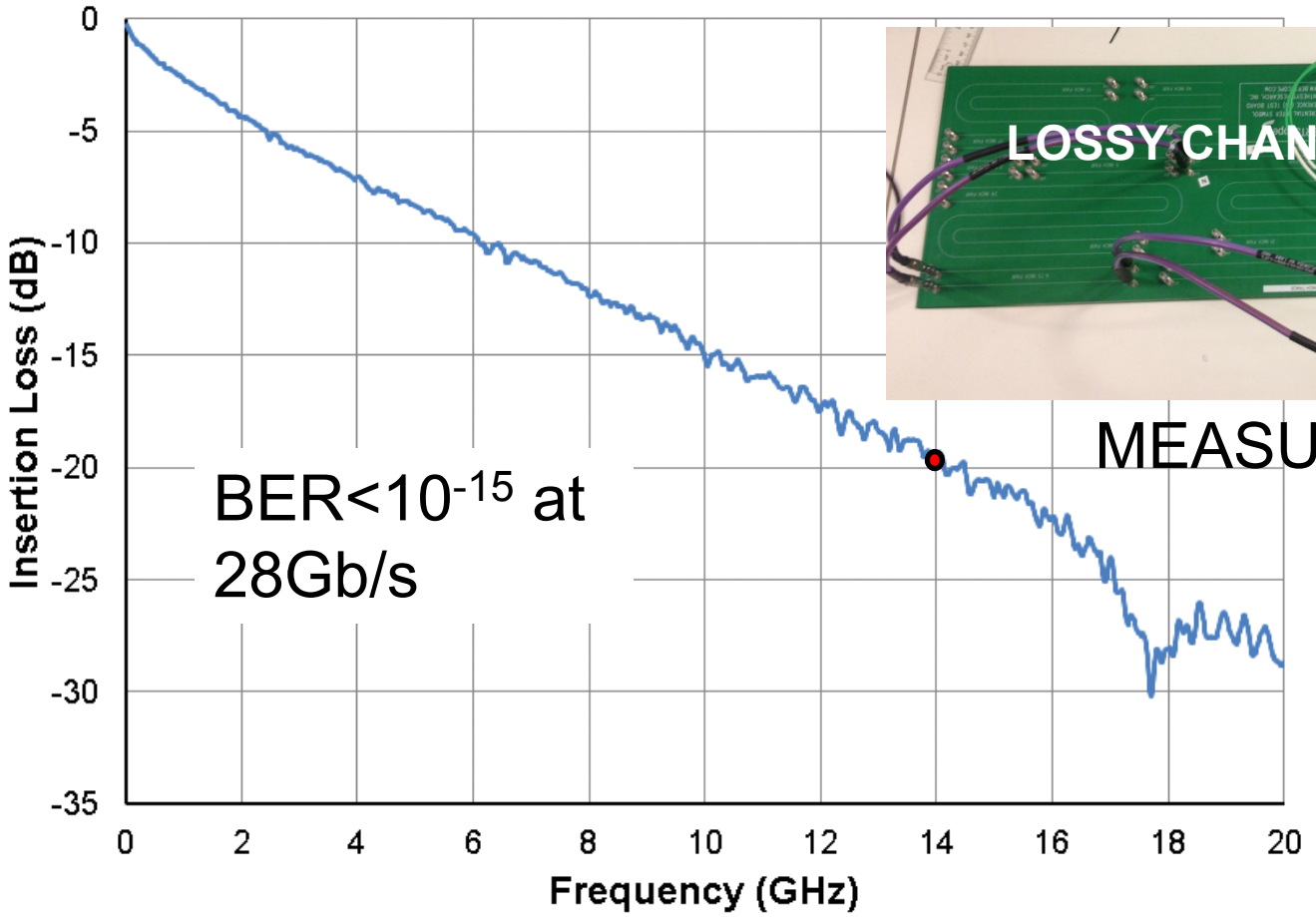
Rise time (20-80%) : 11ps

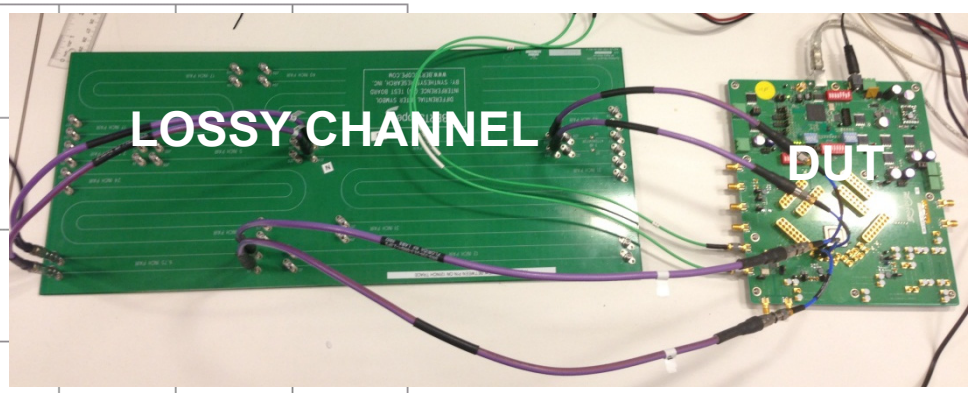
Receiver Jitter Tolerance



- RX input data jitter=11.7ps (0.3UI)
- Measured out-of-band jitter tolerance is 0.46UI_{pp} at 80MHz

RX Equalization Performance



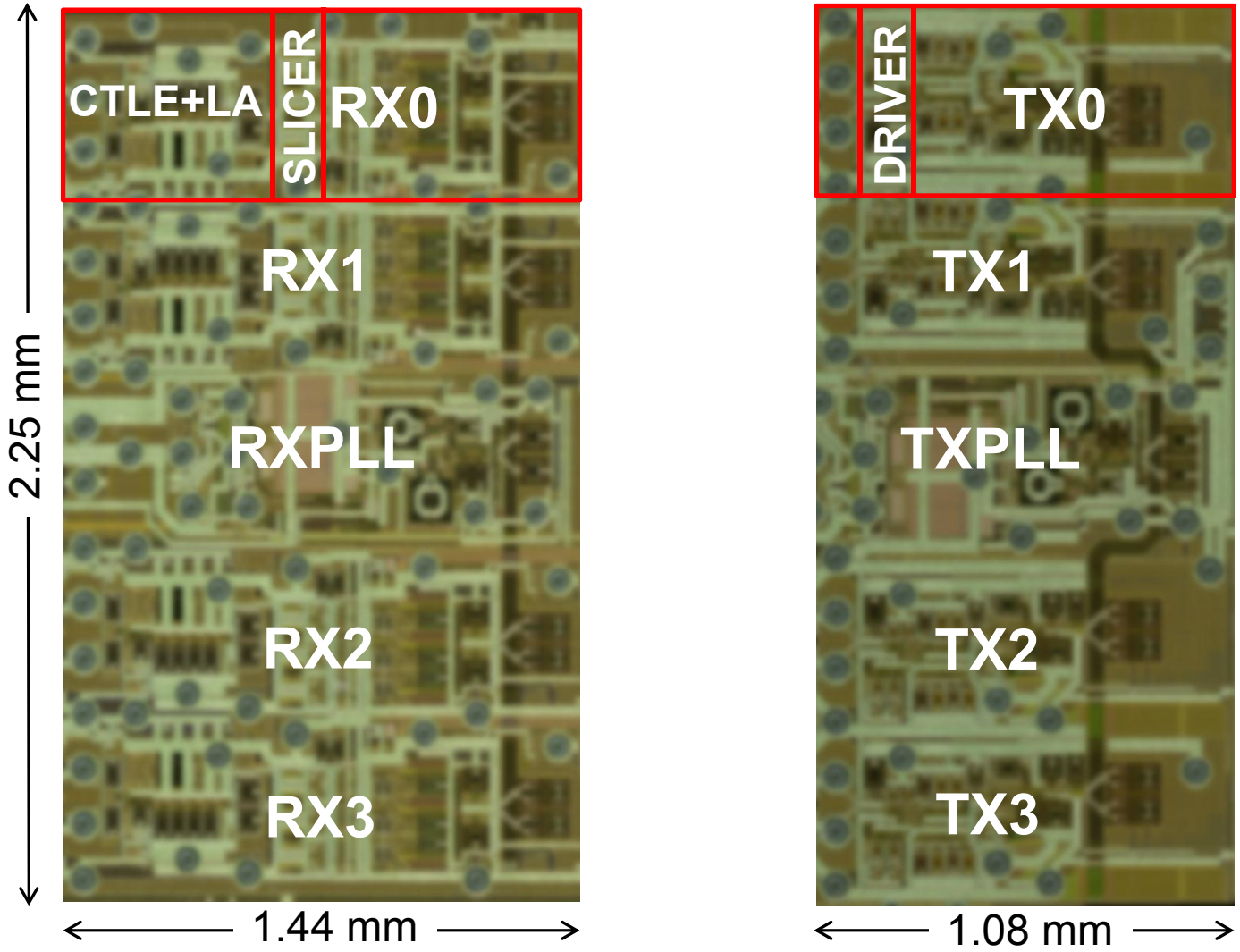


MEASUREMENT SETUP

- 16 inches of Nelco-6000 PCB traces and MMPX cable insertion loss ~ 20dB at 14GHz

Transceiver Die Photo

- 8-metal 40-nm standard digital CMOS process



Outline

- Motivation
- Transmitter
- Receiver
- PLL and Clock Distribution
- Measurement Results
- **Comparison and Summary**

Performance Comparison of 4×28Gb/s Transceiver

		G. Ono ISSCC2011	M. Harwood ISSCC2012	Jhih-Yu Jiang ISSCC2013	This work
Process Technology (CMOS)		65nm	40nm	65nm	40nm
PLL RJ_{rms} (ps)		429fs* (10k to 100MHz)	350fs (100k to 1GHz)	187fs* (100 to 1GHz)	165fs (10k to 100MHz)
TX	DJ_{pp}(ps)	3.3*	NA	NA	1.87
	TJ_{pp} (ps) BER= 10^{-12}	NA	NA	6.67*	4.63
RX Jitter Tolerance (UI_{pp}) @ 80MHz		NA	0.4	0.2*	0.46
RX Input Sensitivity ($mV_{pp\text{-}diff}$)		34.4*	NA	NA	27
Compensated channel loss (dB) @ Nyquist (BER = 10^{-15})		NA	13	NA	20
Power Supply		1/1.8V	NA	1.2V	0.9V
Power of 4×28G Interface (W)		1.4*	0.9	1.84*	0.78
Supported Data Rate (Gb/s)		25	25 to 28	25	20 to 28

* Measured at 25.78Gb/s.

Conclusion

- A low-power reconfigurable 4×28Gb/s transceiver is demonstrated
- Low Power is achieved by:
  - *Controlled swing low-jitter transmitter*
  - *Calibrated RX slicer with active inductor*
  - *Dual VCO PLL*
  - *Distributed programmable tuned clock driver*
- The PHY shows best in class performance and surpasses ITU OTL-4.4 and 28G VSR specifications

Acknowledgement

The authors would like to thank the support of the Broadcom DSP, ASIC and Layout groups in AFE design and the DVT groups for the measurement.

Paper 2.3

60Gb/s NRZ and PAM4 Transmitters for 400GbE in 65nm CMOS

Ping-Chuan Chiang, Hao-Wei Hung,

Hsiang-Yun Chu, Guan-Sing Chen, Jri Lee

Electrical Engineering Department

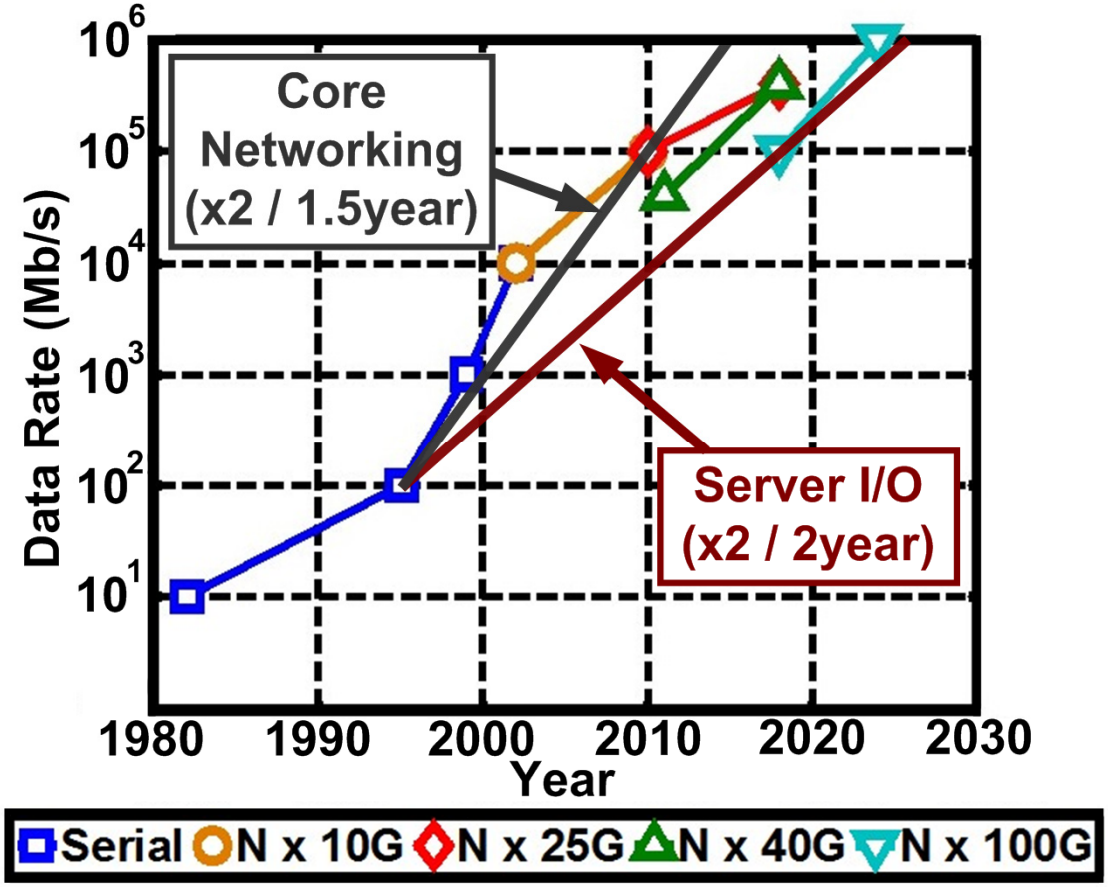
National Taiwan University

Outline

- Introduction
- Architecture
- Building Blocks
- Experimental Results
- Conclusion

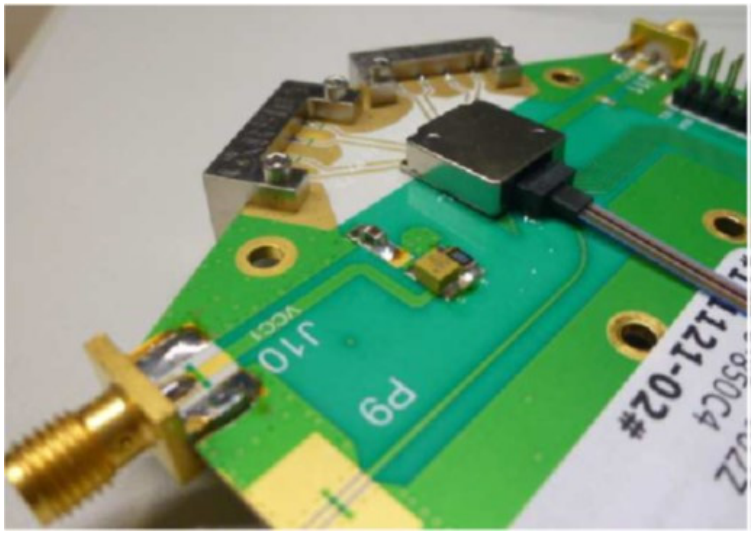
400Gb/s Ethernet

Data Rates of Ethernet



(Ref: Ethernet Alliance)

100GbE Test Board

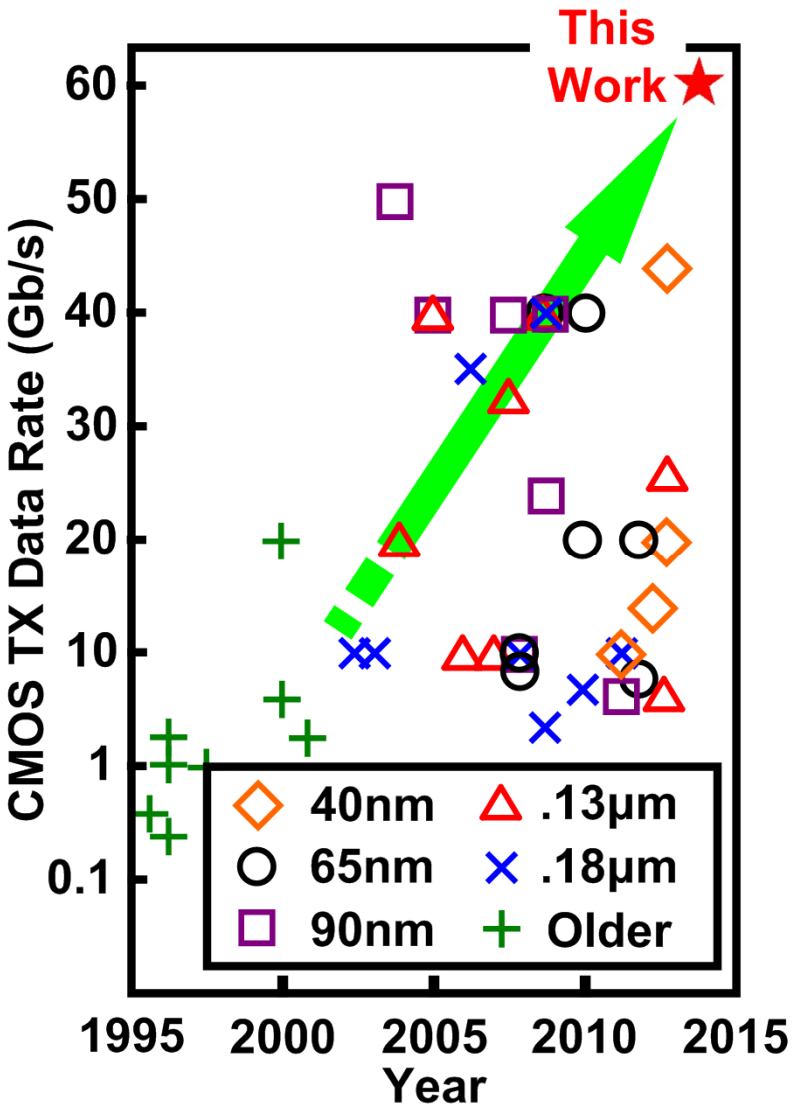


- 4x25Gb/s Data Rate
- 850nm VCSEL
- PIN Photo Detector
- 3.3V Supply Voltage

(Ref: VI System)

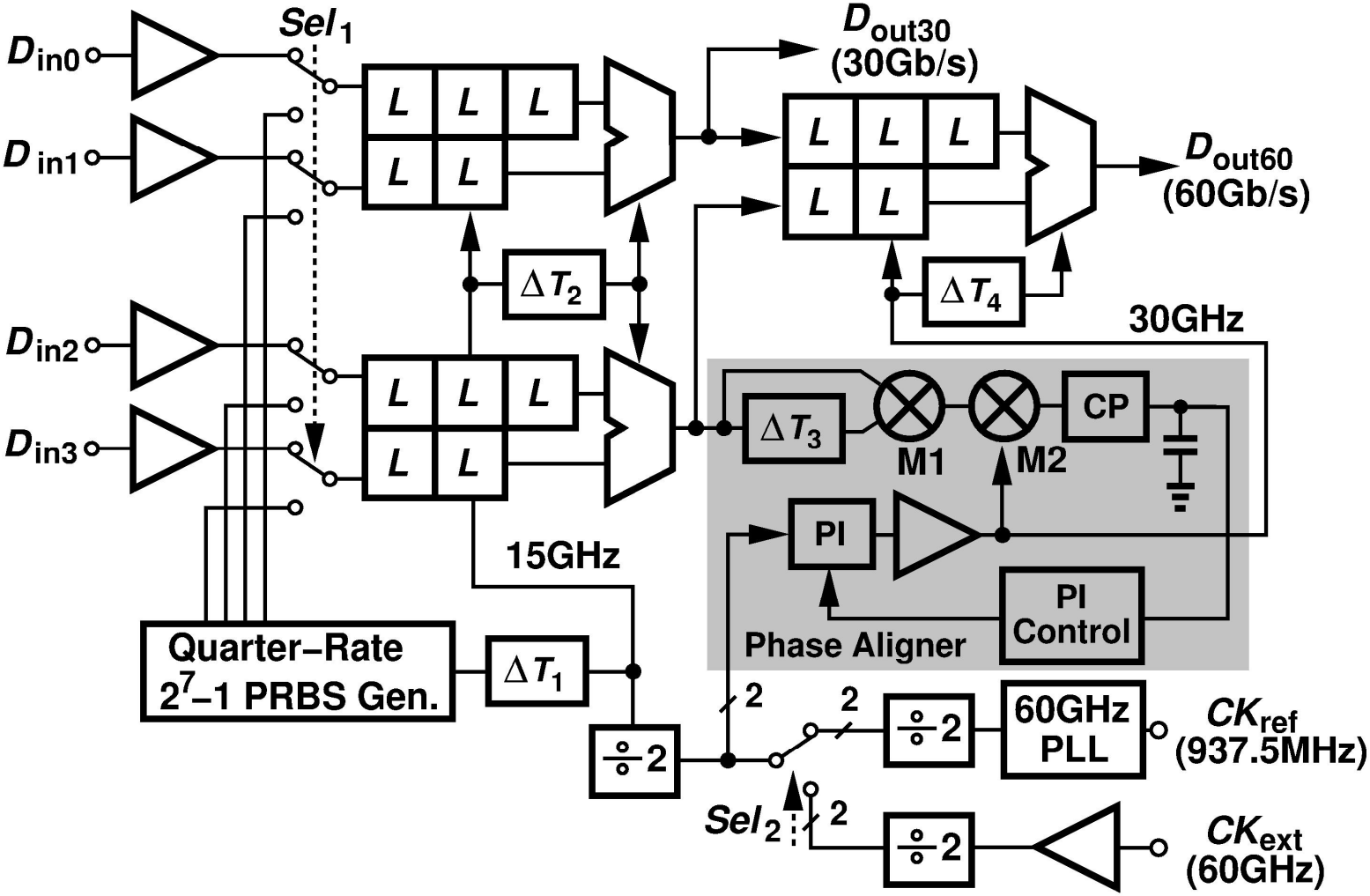
400Gb/s Ethernet

- **8x25GB/s PAM4 (Short Term)**
  - New modulation format
  - Duplex SMF/Parallel SMF
  - Need FEC for 2km application
- **8x50Gb/s NRZ (Long Term)**
  - Current TX distance~2km
  - Expensive devices
- **IEEE 802.3 400GbE Study Group**
  - 5” daughter card trace
  - 40km transmission distance



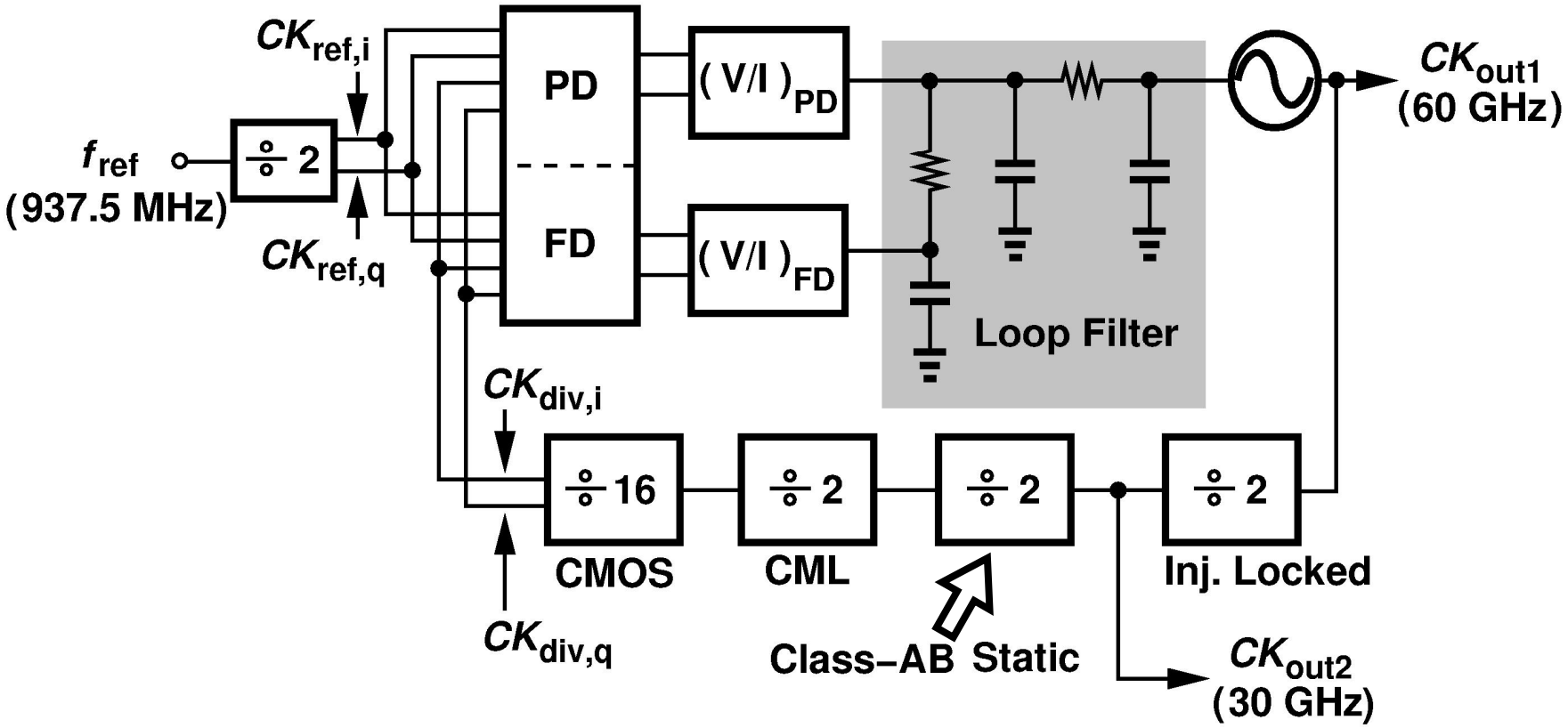
➪ **New era of ultra high-speed data link is coming!**

NRZ TX Architecture



- Built-in PRBS generation
- Dual operation modes
- Phase aligner to track the optimal clock phase

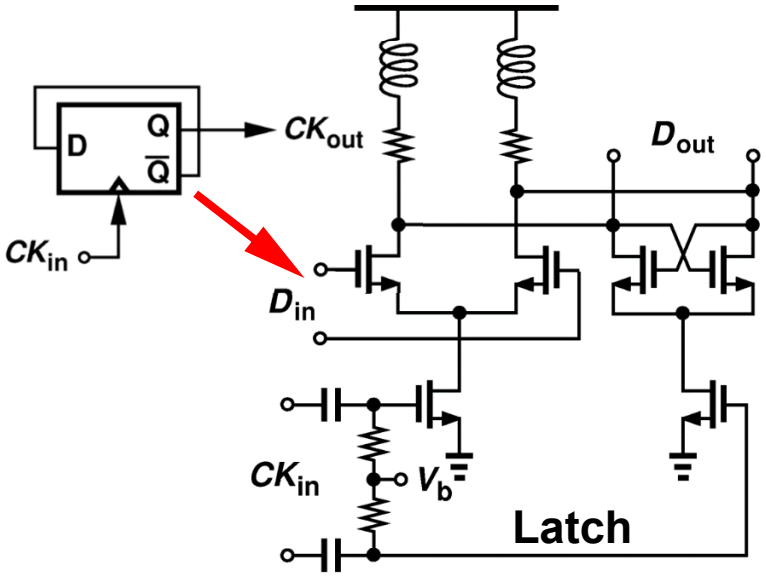
NRZ TX Clock Generation



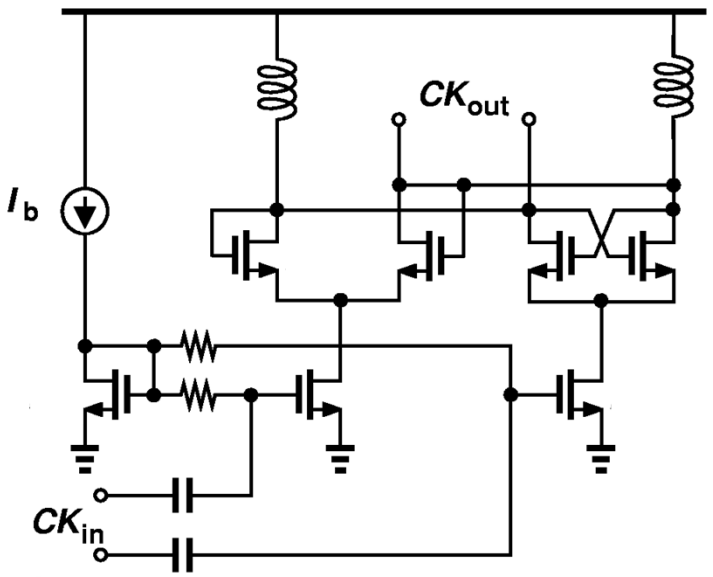
- Improvement from [Lee, '07]
  - Minimize power
  - 30% Smaller area
  - Replace Miller divider by a class-AB divider

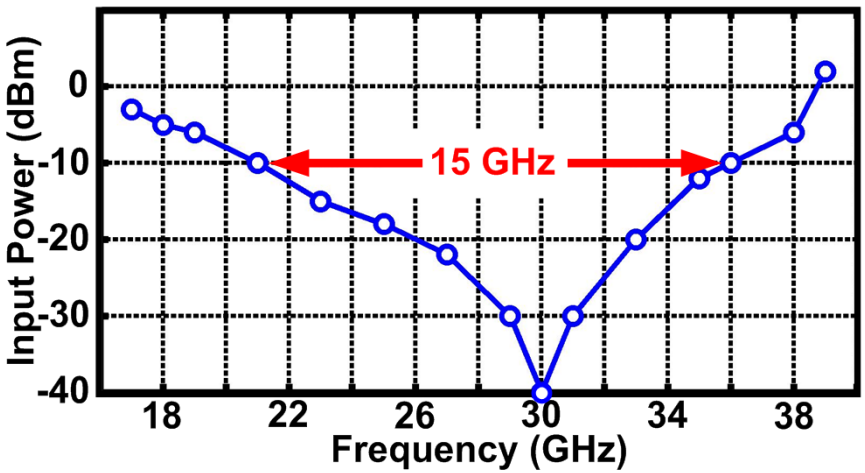
Class-AB Biased Static v.s. Miller Dividers

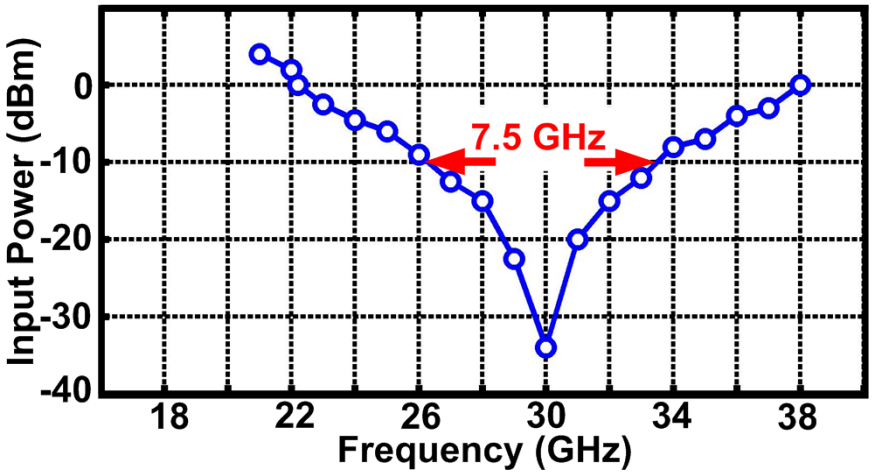
❒ Class-AB Biased



❒ Miller



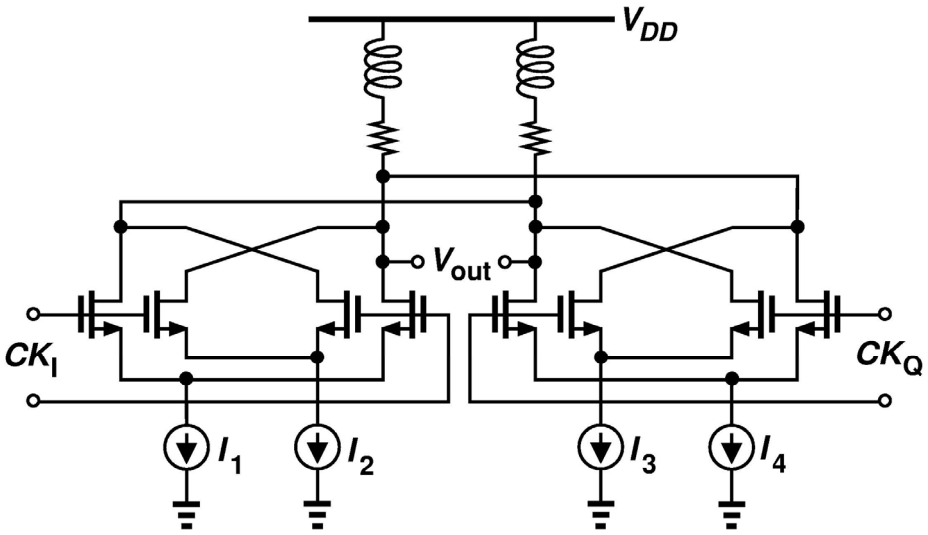


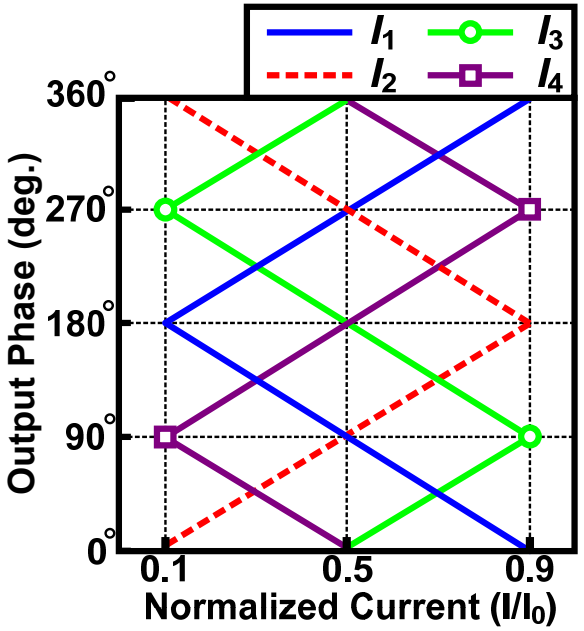


➪ Operation range increases from 7.5 to 15 GHz

Phase Aligner

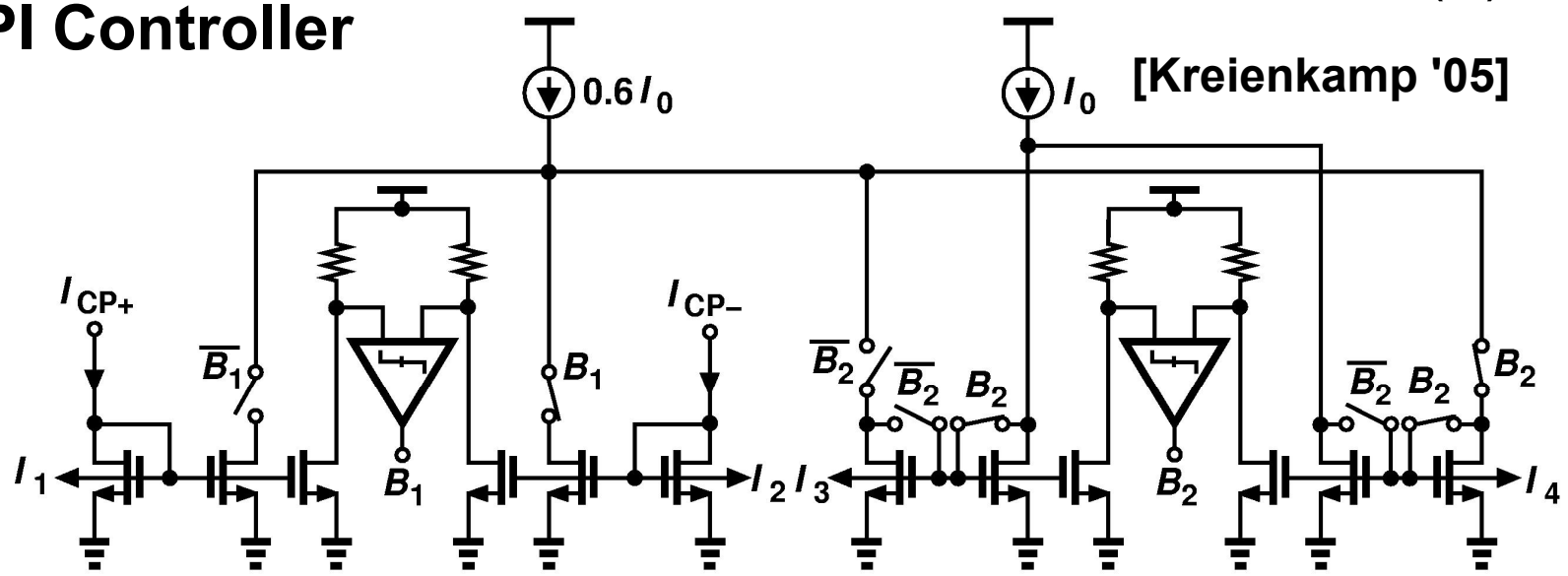
Phase Interpolator



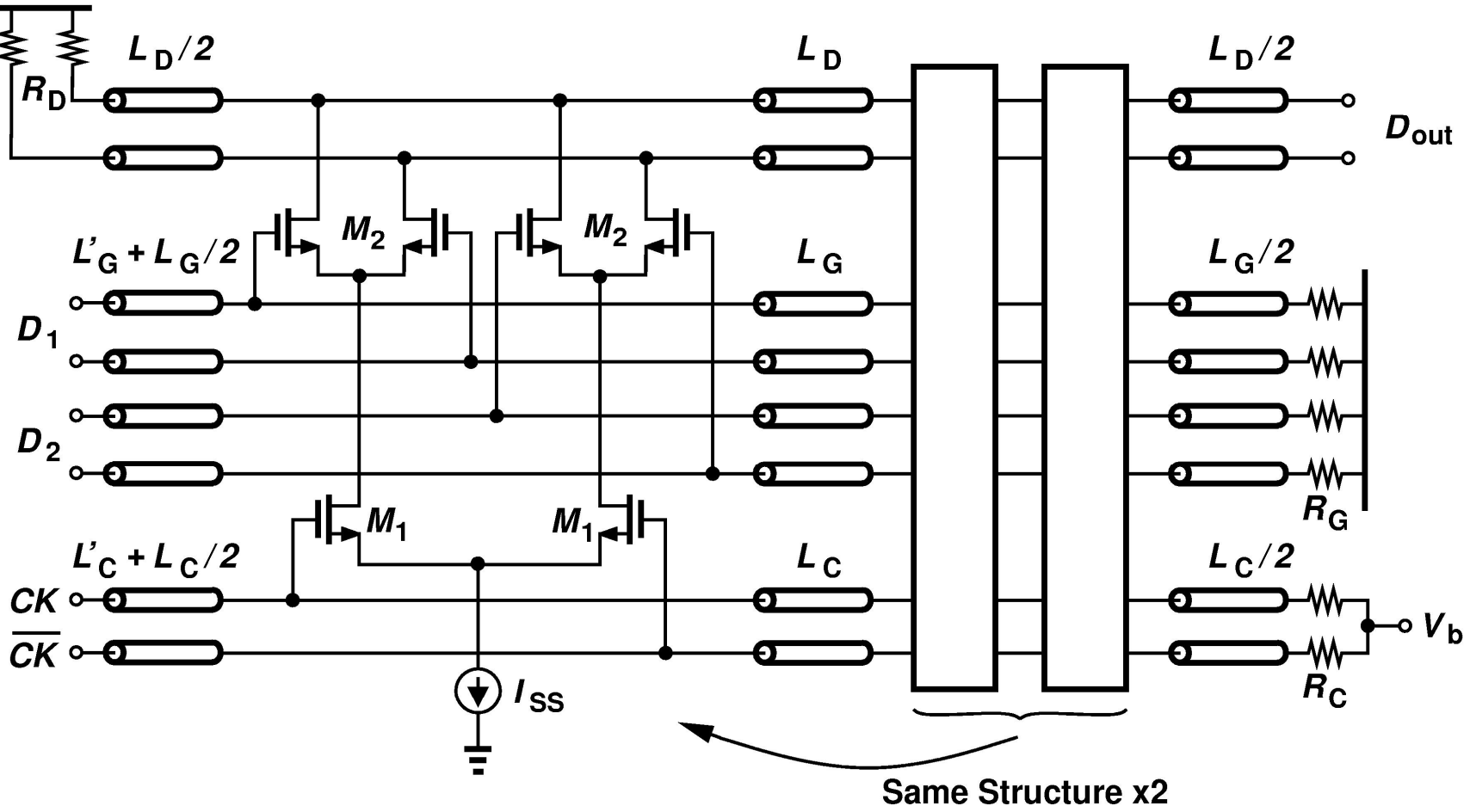


PI Controller

[Kreienkamp '05]



60Gb/s MUX

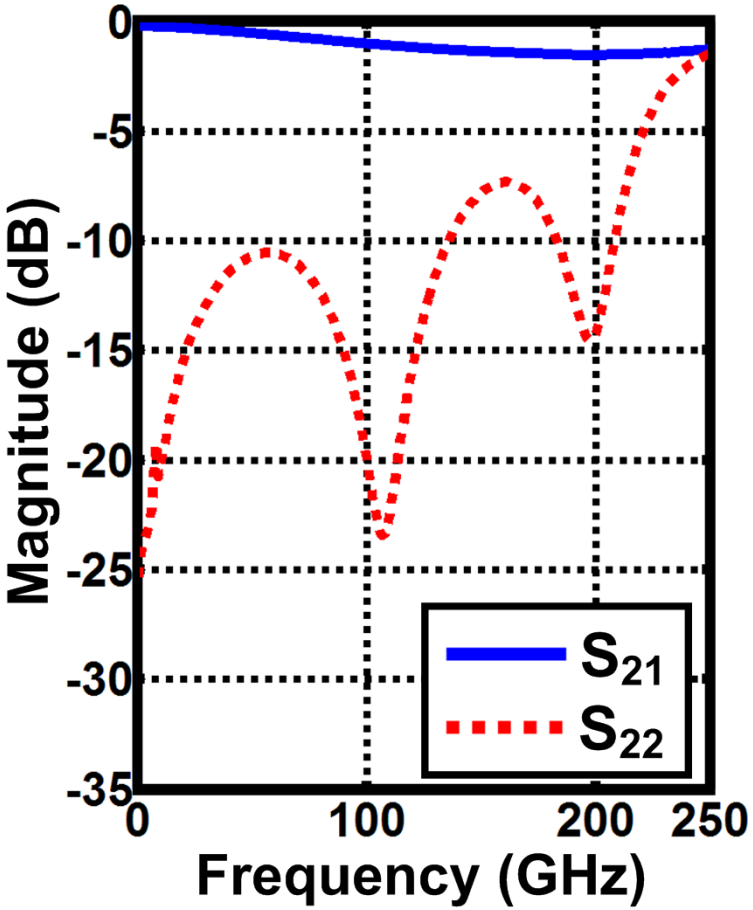


M_1	M_2	R_D, R_G, R_C	I_{SS}	L_G, L_C	L_D
30/0.06	24/0.06	50Ω	7mA	105pH	W = 4um L = 210um

- Distributed MUX [Singh '06]
- T-Line improves bandwidth from 34Gb/s to 60Gb/s

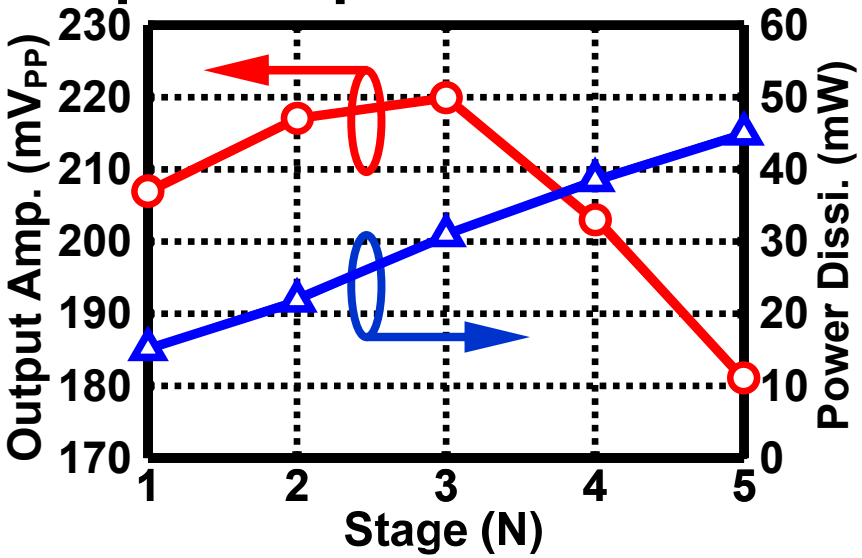
60Gb/s MUX

S-Parameters

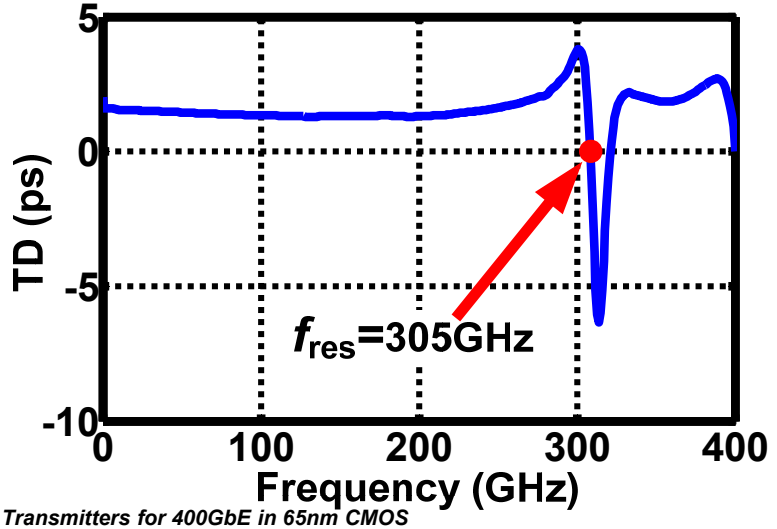


- Broadband matching
- 1.5dB loss @ 60GHz

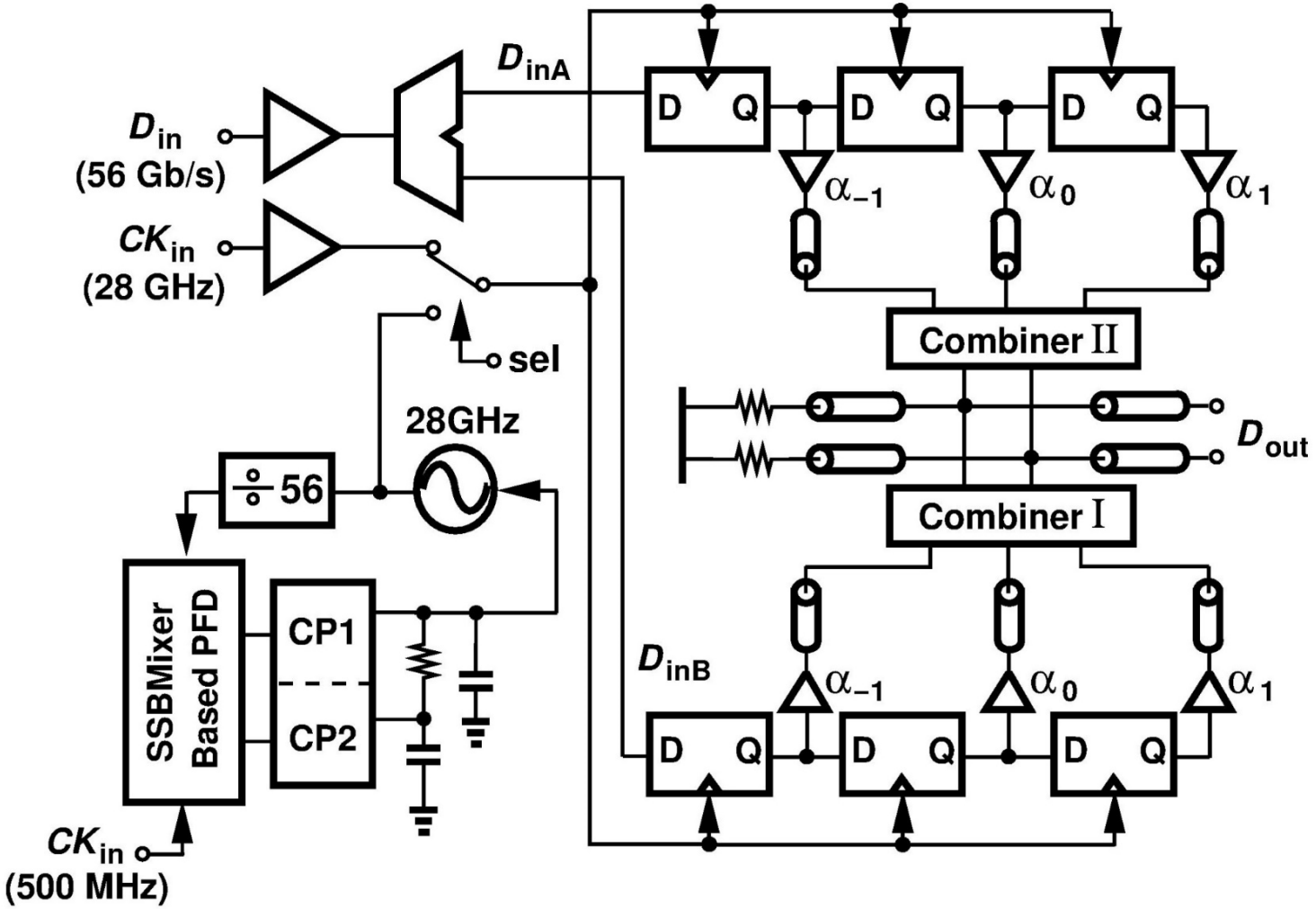
Output Amplitude v.s. Power



Propagation Delay

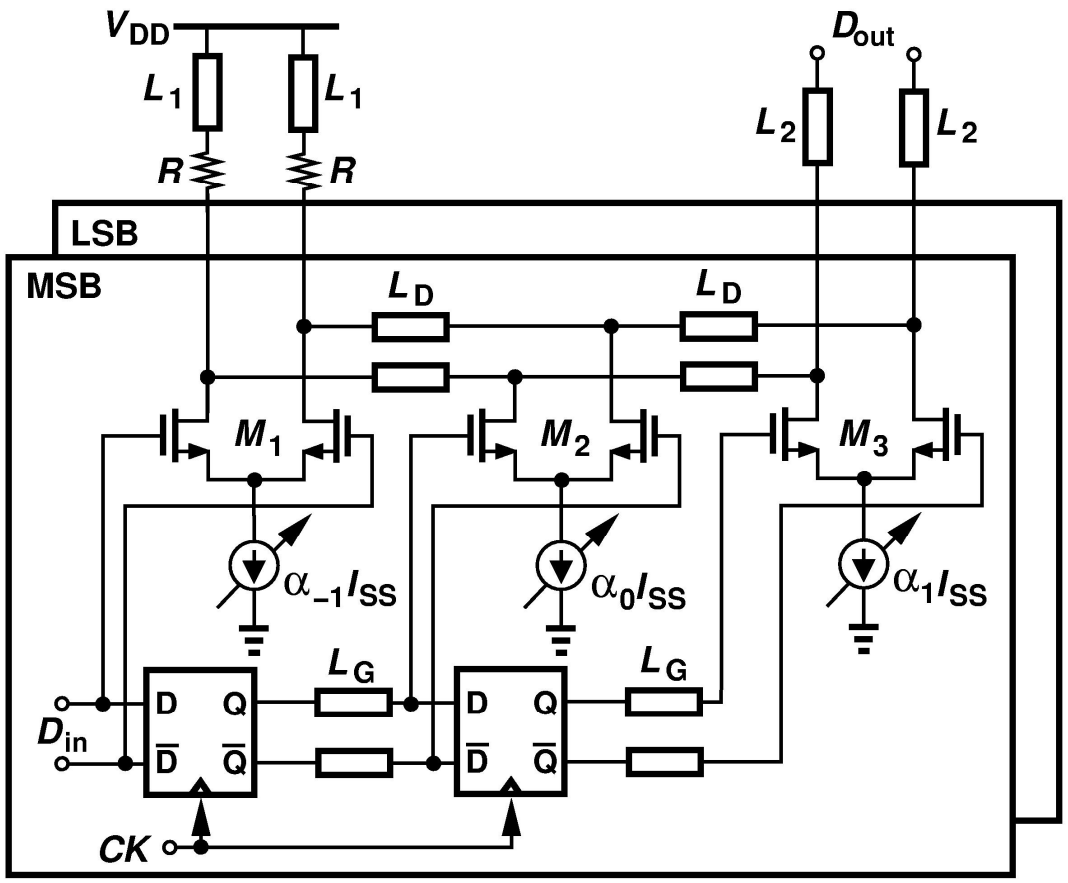


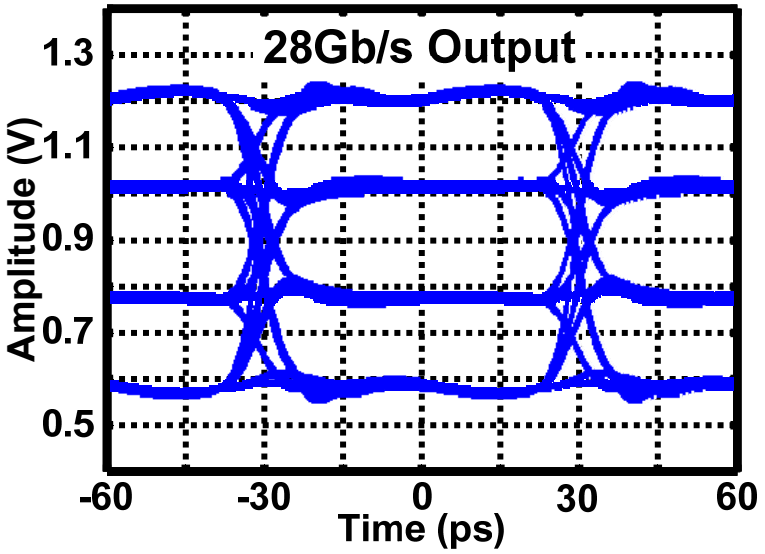
PAM4 TX Architecture

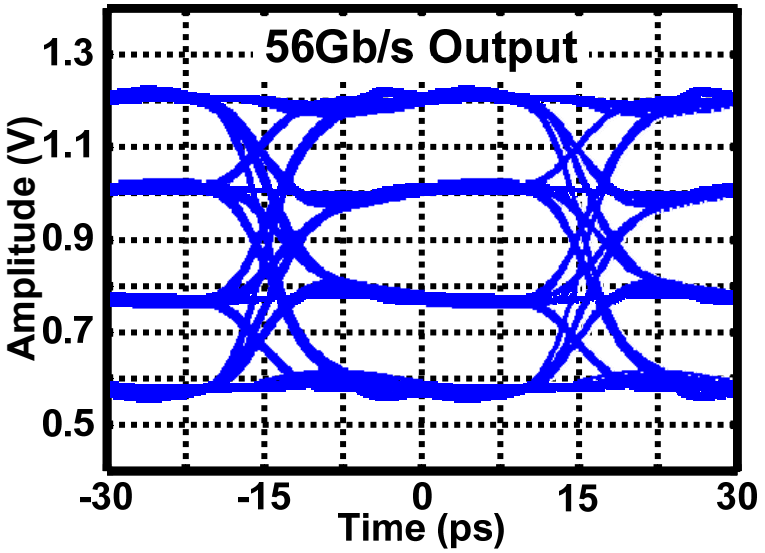


- Built-in Synthesizer
- 3-tap FFE as output driver
- 1-62Gb/s wide-range operation by external clocking

Combiner





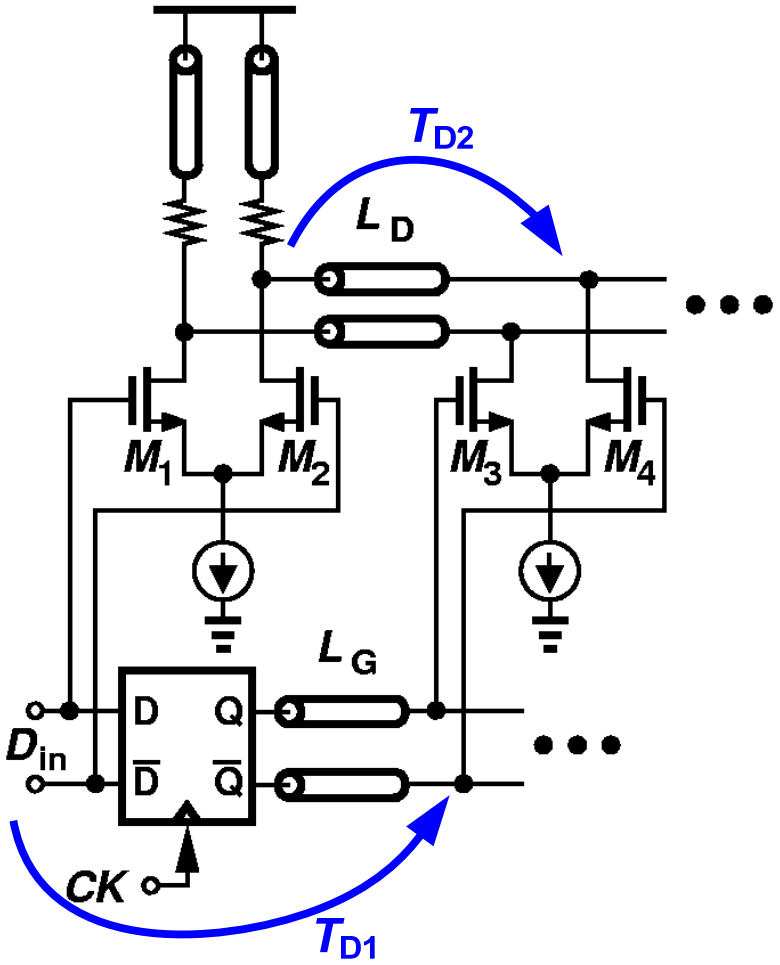


M_1	M_2	M_3	R	L_D	L_G	$L_{1\text{-}2}$	I_{SS}
4 / 0.06	48 / 0.06	4 / 0.06	60Ω	W = 4 L = 105	W = 2 L = 40	130pH	12mA

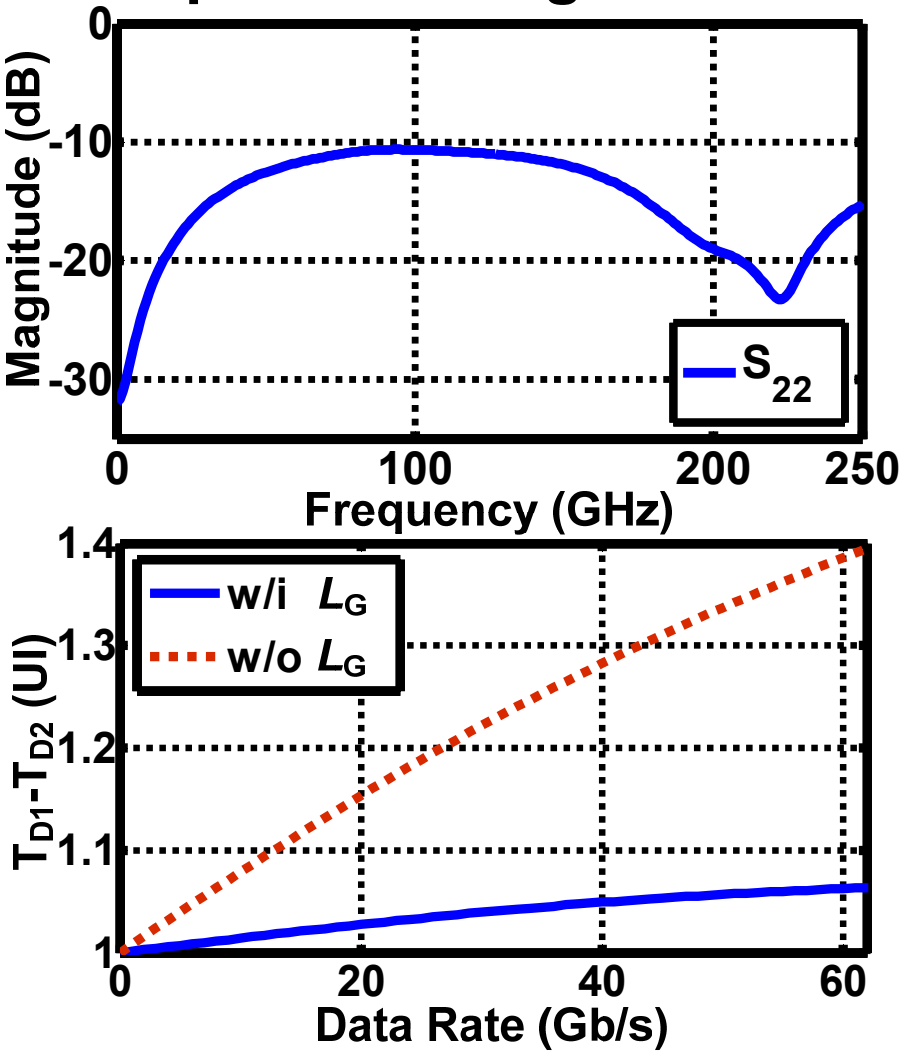
- CML combiner provides stable operation up to 62Gb/s

Combiner

❒ Propagation Delay

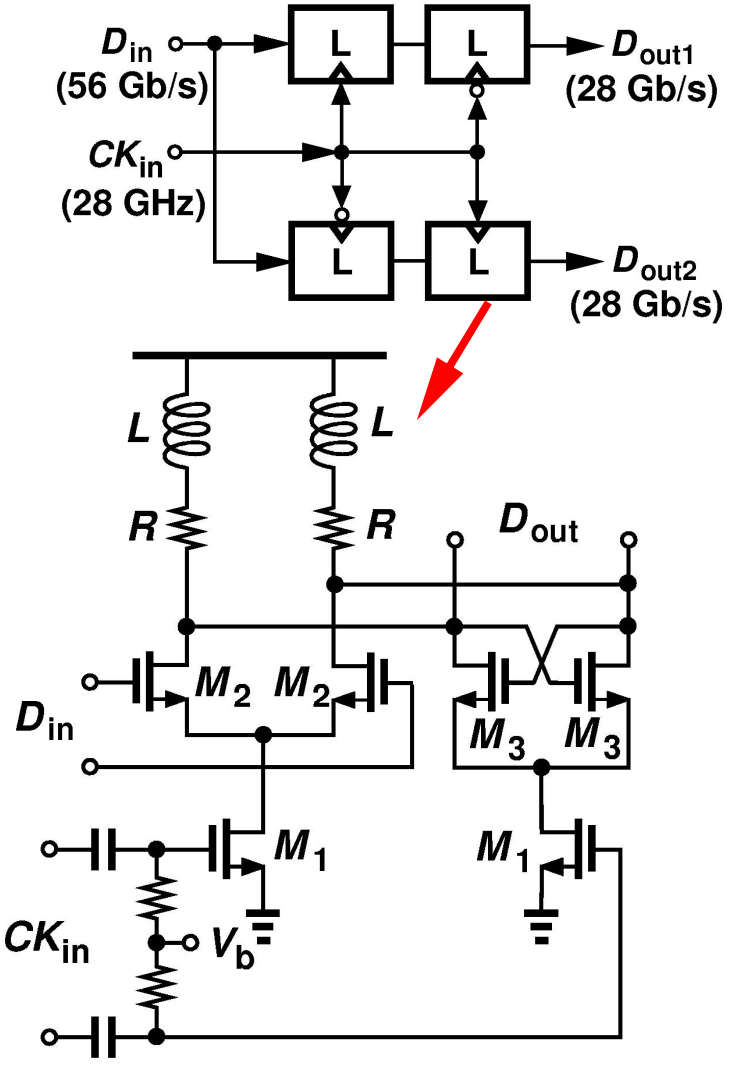


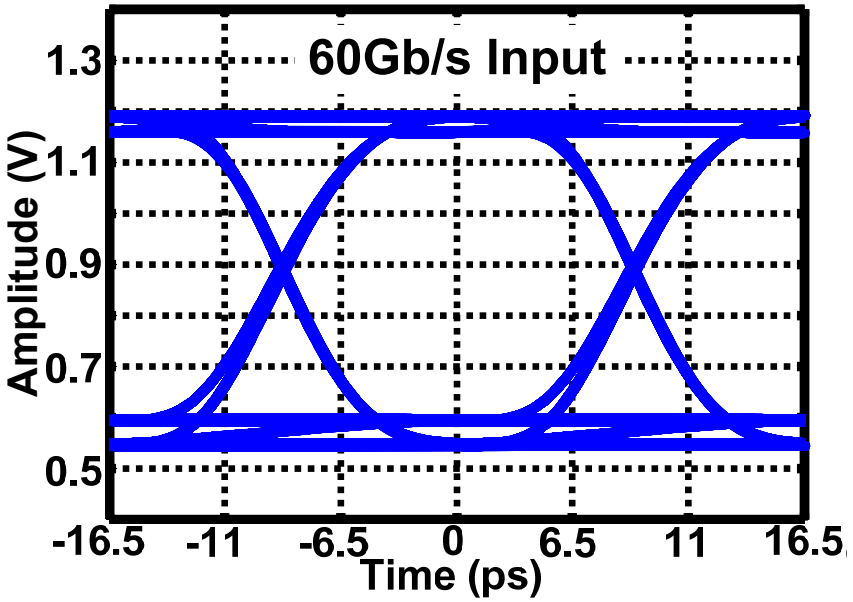
❒ Output Matching

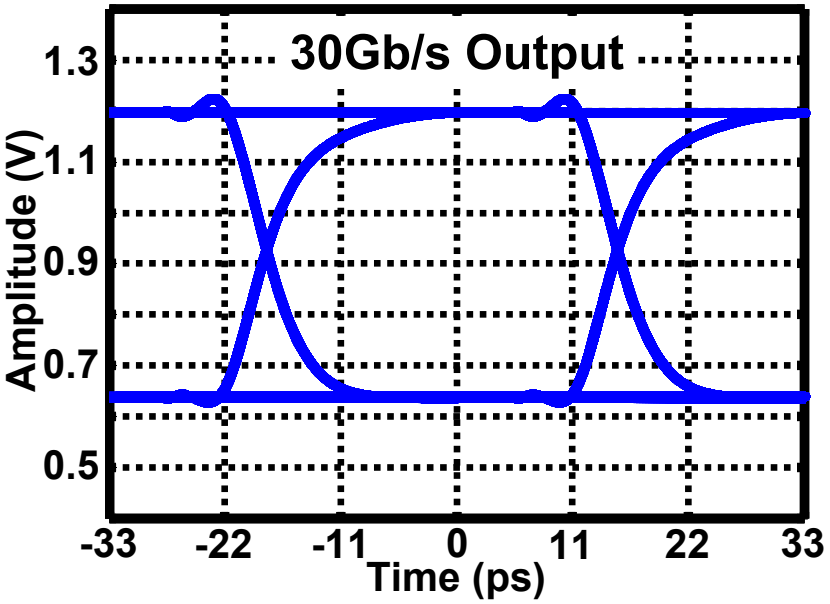


- L_G improves 0.3UI eye opening @ 60Gb/s

Demultiplexer

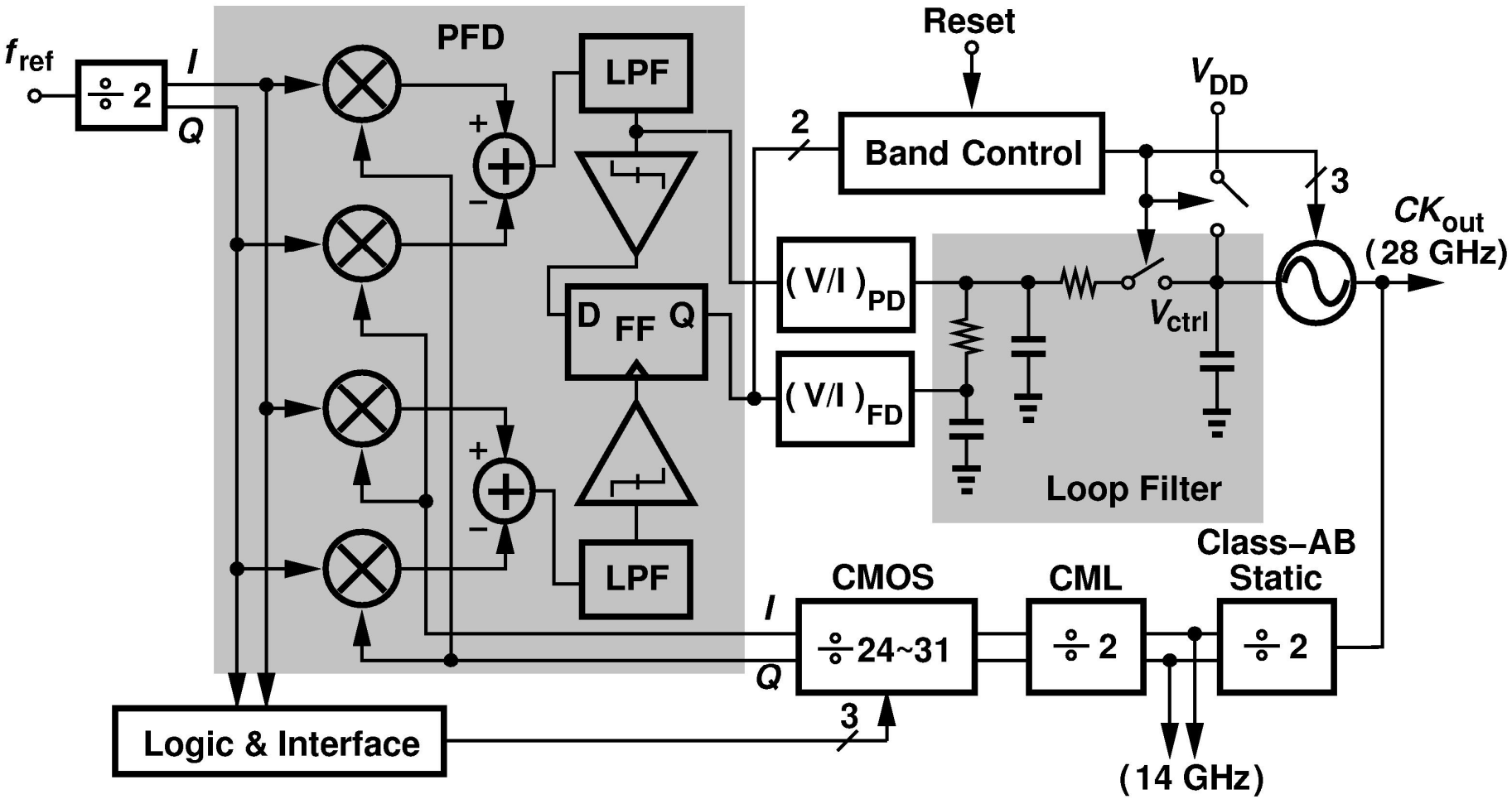






- **Operation range = 1~62Gb/s**

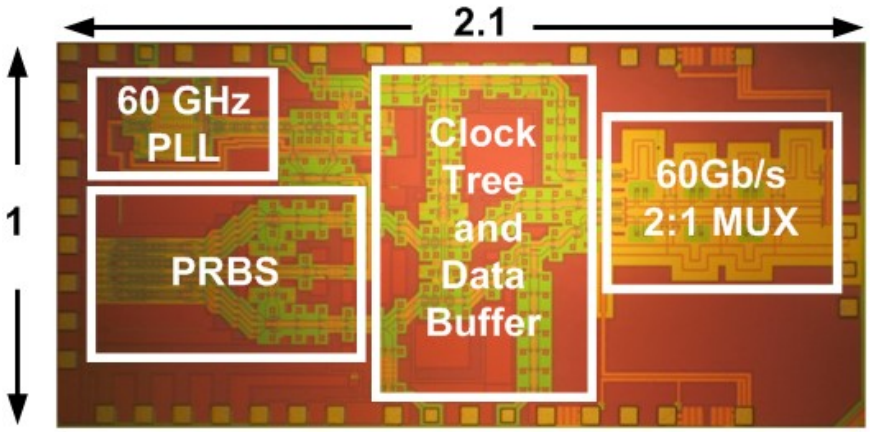
PAM4 TX Clock Generation

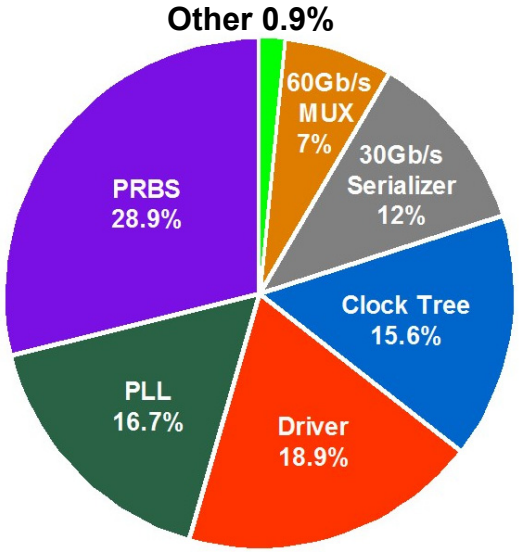


- Mixer-based PFD [Lee, '07]
- Band-controlled logic
- Operation range = 26.2~31.5GHz

Chip Micrograph

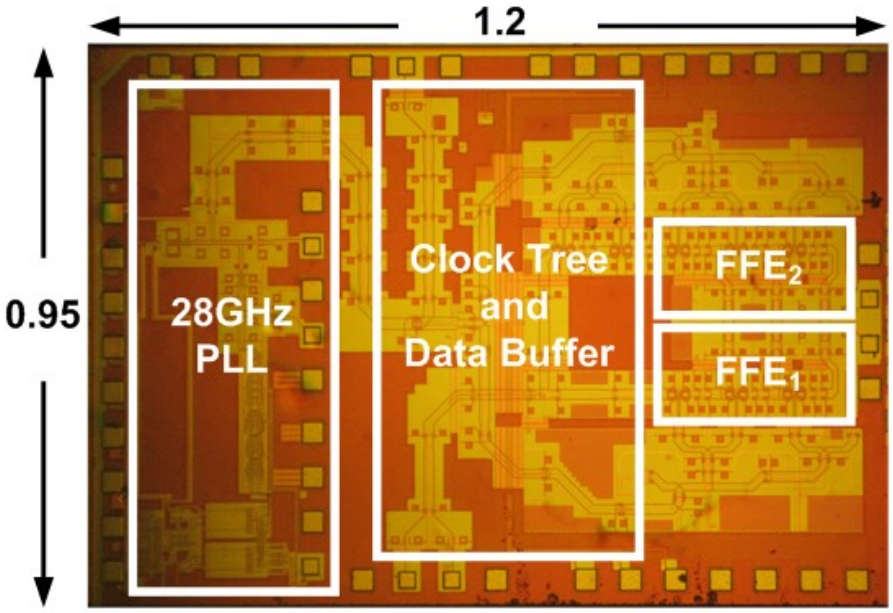
❒ NRZ TX (Unit: mm)

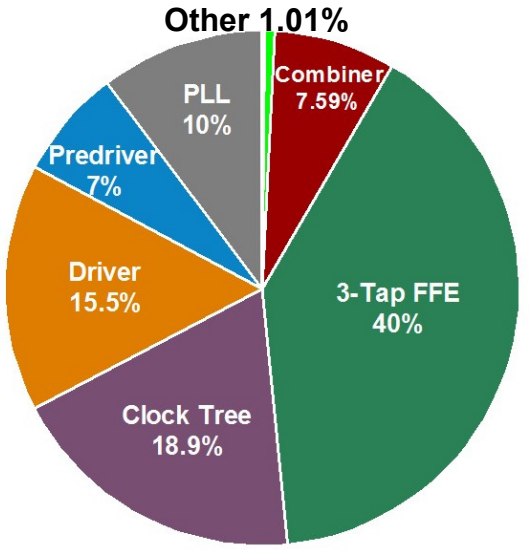




Total Power: 450mW

❒ PAM4 TX

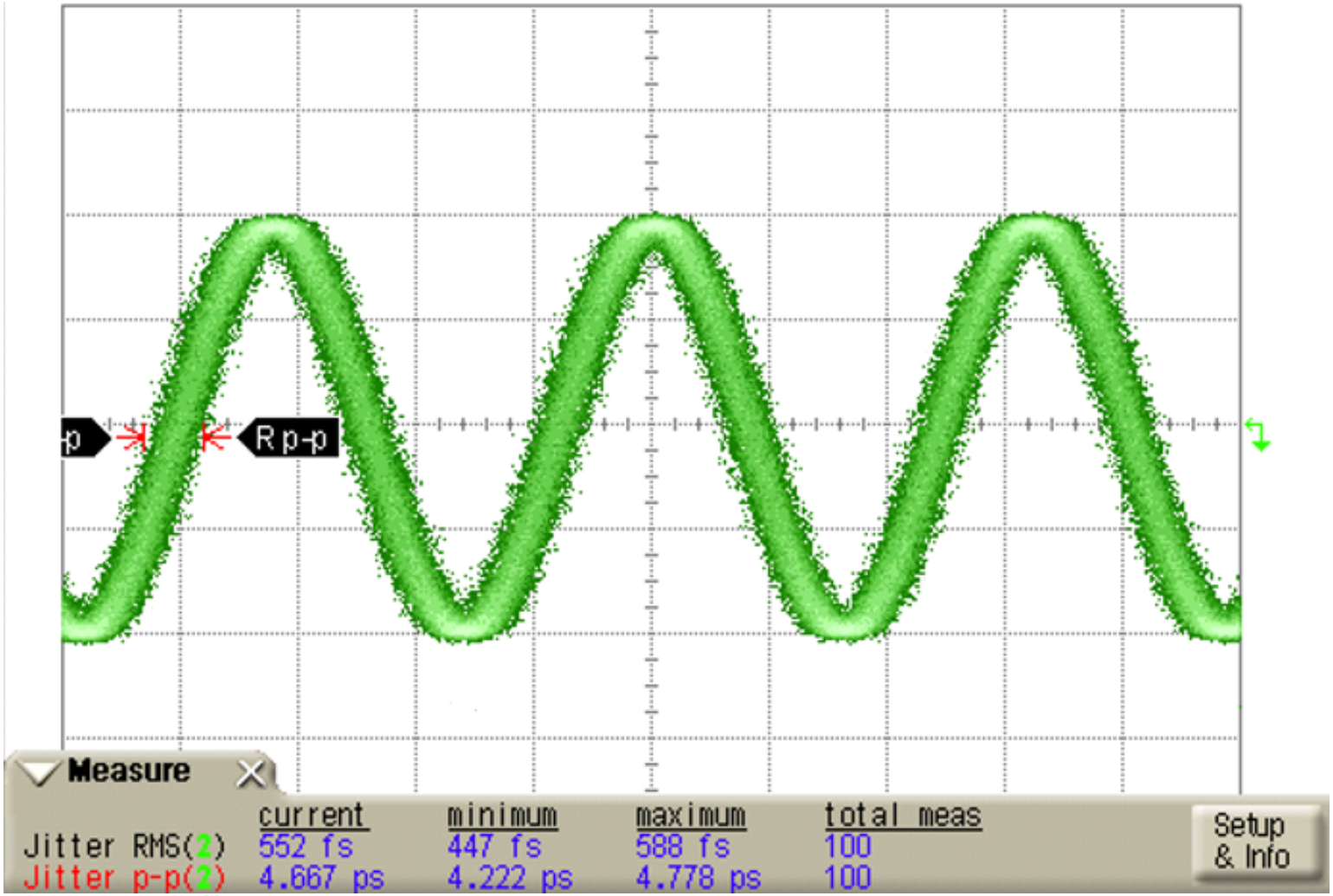




Total Power: 290mW

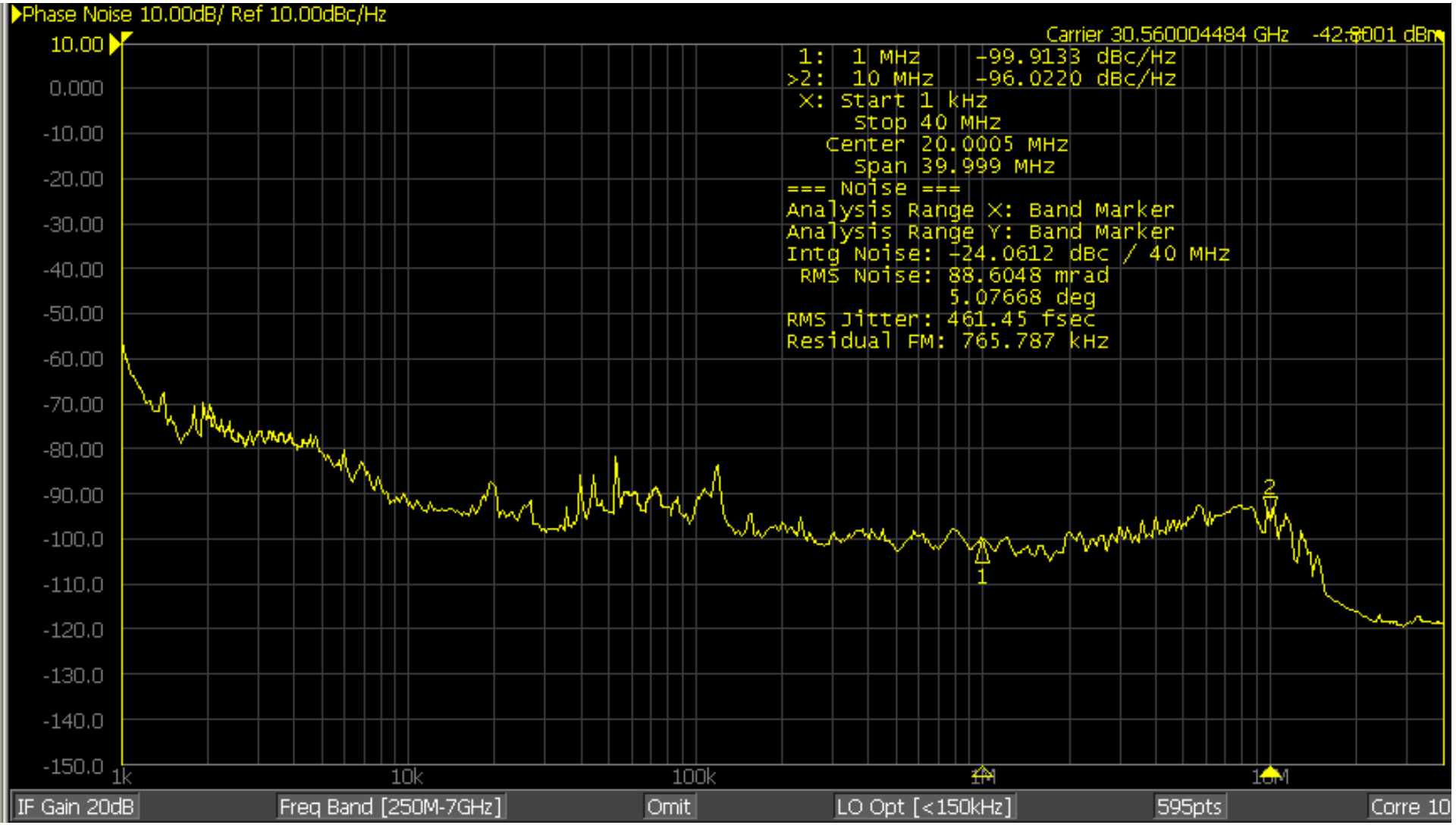
NRZ TX PLL Measurement

- 30GHz Output



- Clock Jitter = 461 fs,rms/4.67 ps,pp

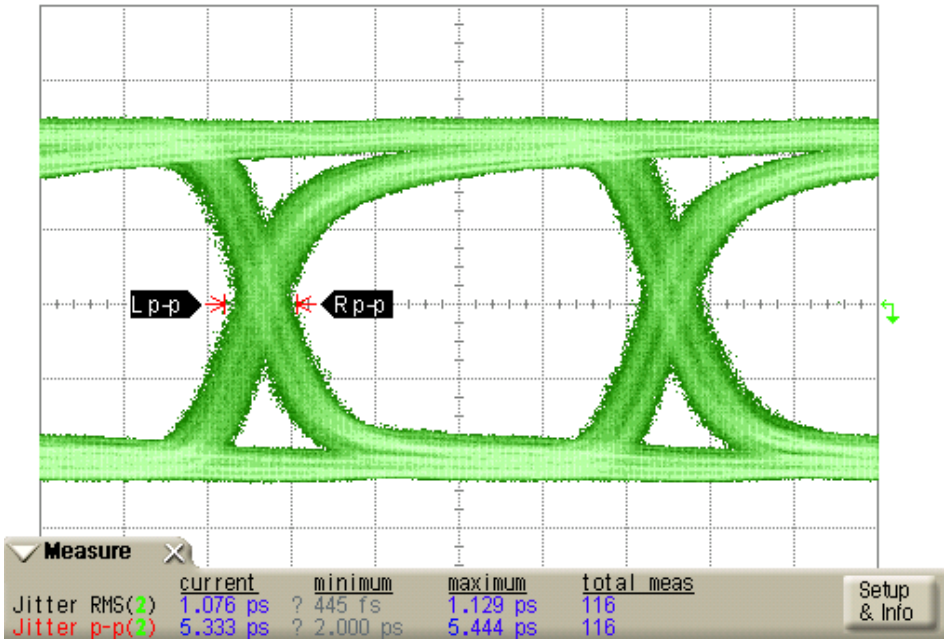
NRZ TX Clock Phase Noise



- **Phase Noise = –100dBc/Hz @ 1MHz offset**

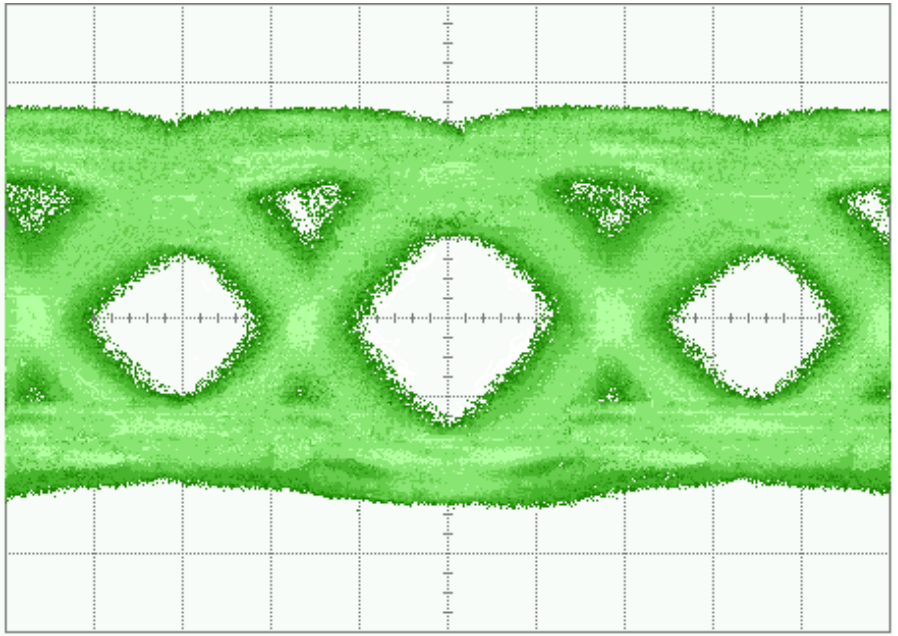
NRZ TX Data eyes

- 30Gb/s Output



RMS Jitter = 1.08ps
Peak-Peak Jitter = 5.33ps
Vertical: 50mV/div
Horizontal: 6.5ps/div

- 60Gb/s Output

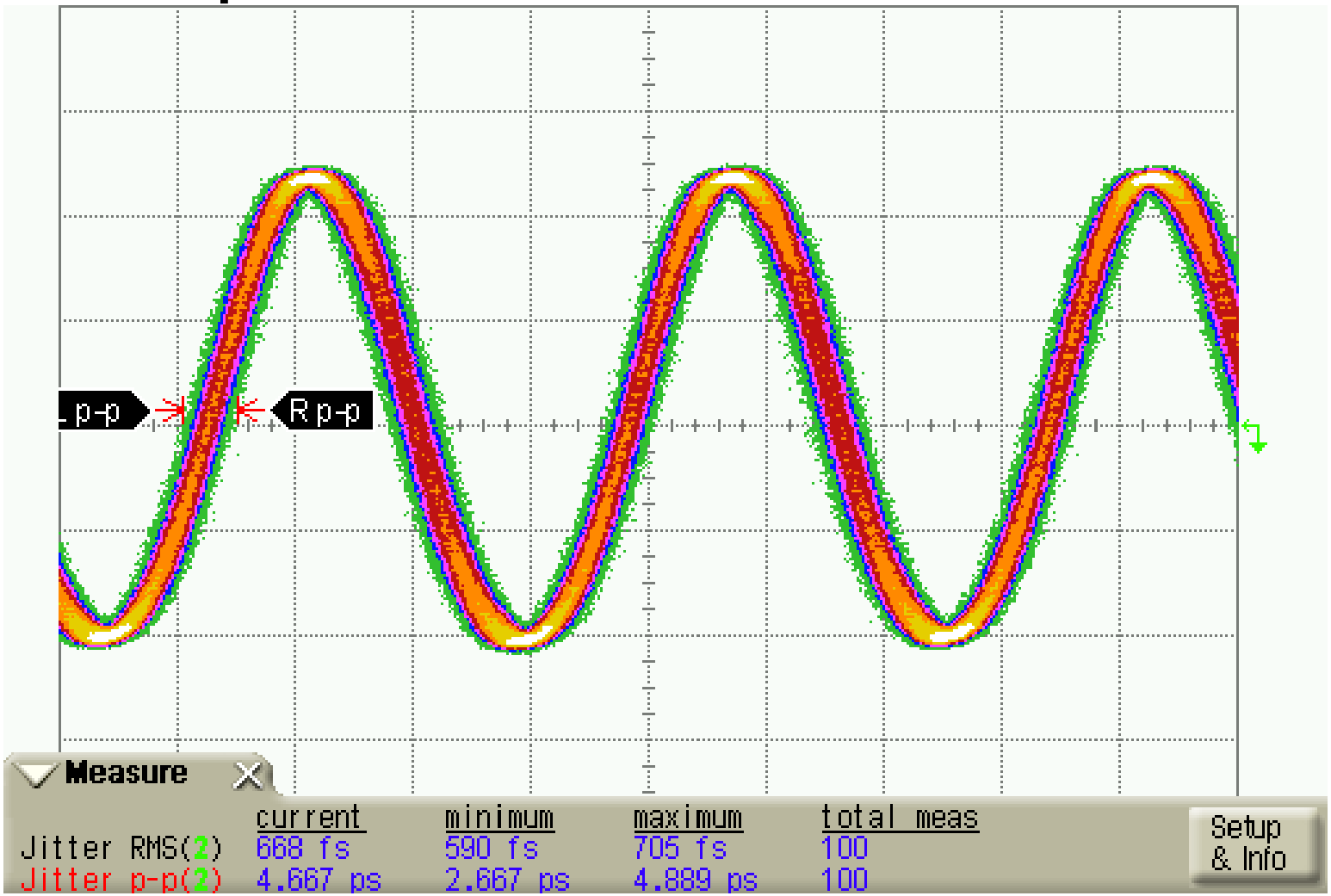


Vertical: 50mV/div
Horizontal: 5ps/div

***60Gb/s Data jitter is not captured due to limited oscilloscope bandwidth**

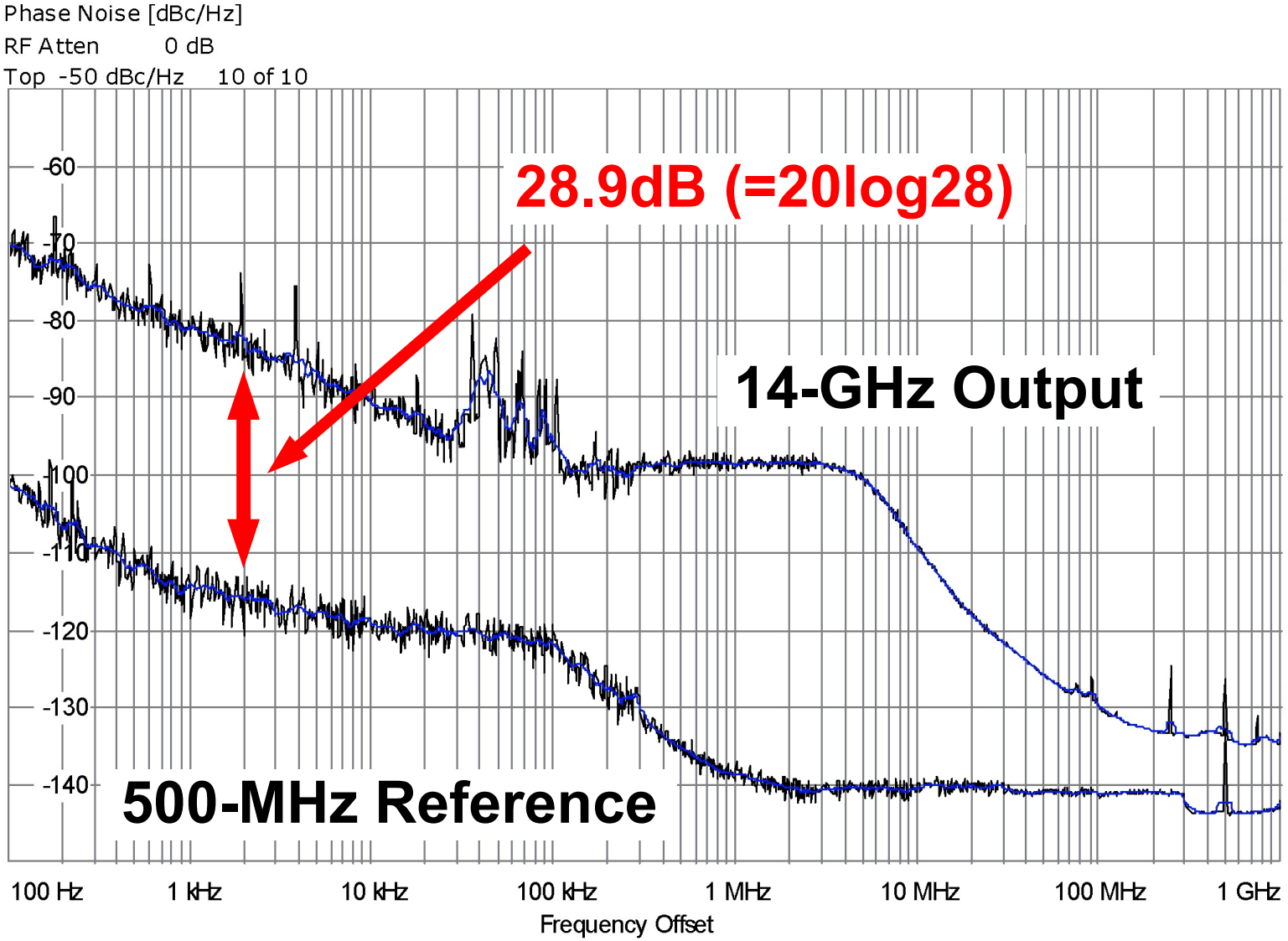
PAM4 TX PLL Measurement

- 28GHz Output



- Clock Jitter = 508 fs,rms/4.67 ps,pp

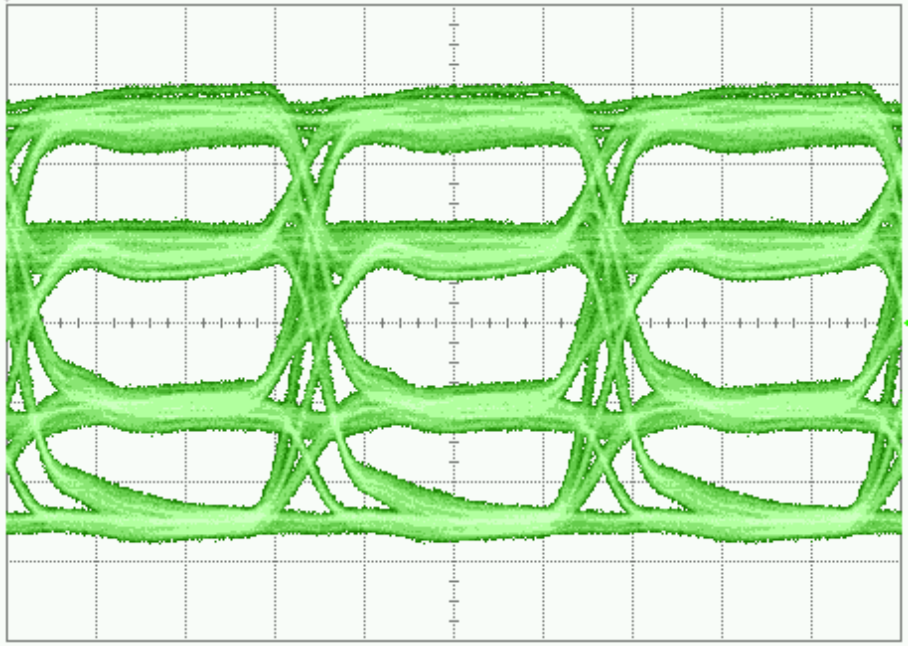
PAM4 TX Clock Phase Noise



- Phase Noise = –98.5dBc/Hz @ 1MHz offset

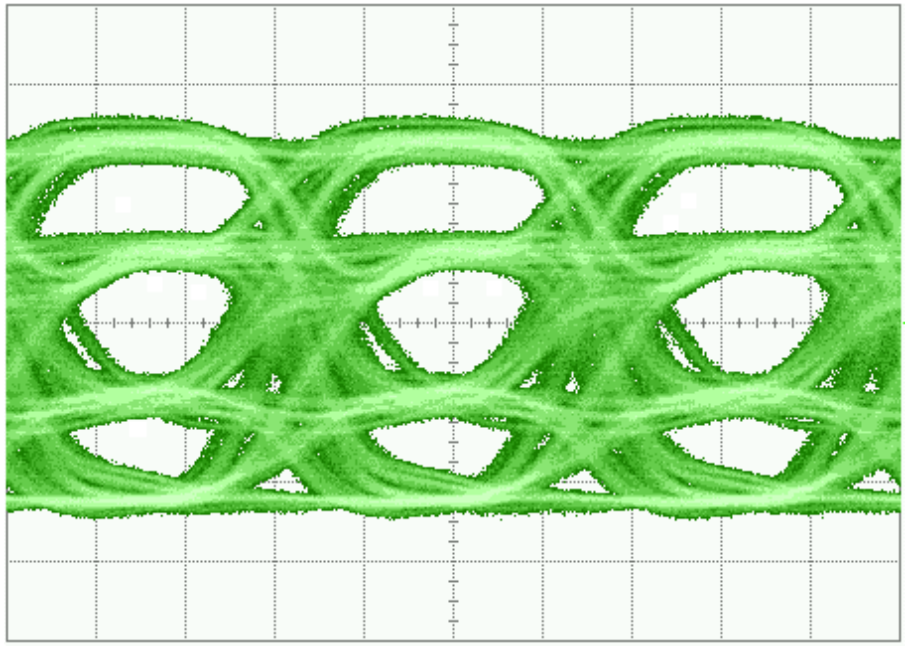
PAM4 TX Data eyes

- 30Gb/s Output



Level Spacing = 50mV
Horizontal Opening = 0.80UI
Vertical: 50mV/div
Horizontal: 20ps/div

- 60Gb/s Output

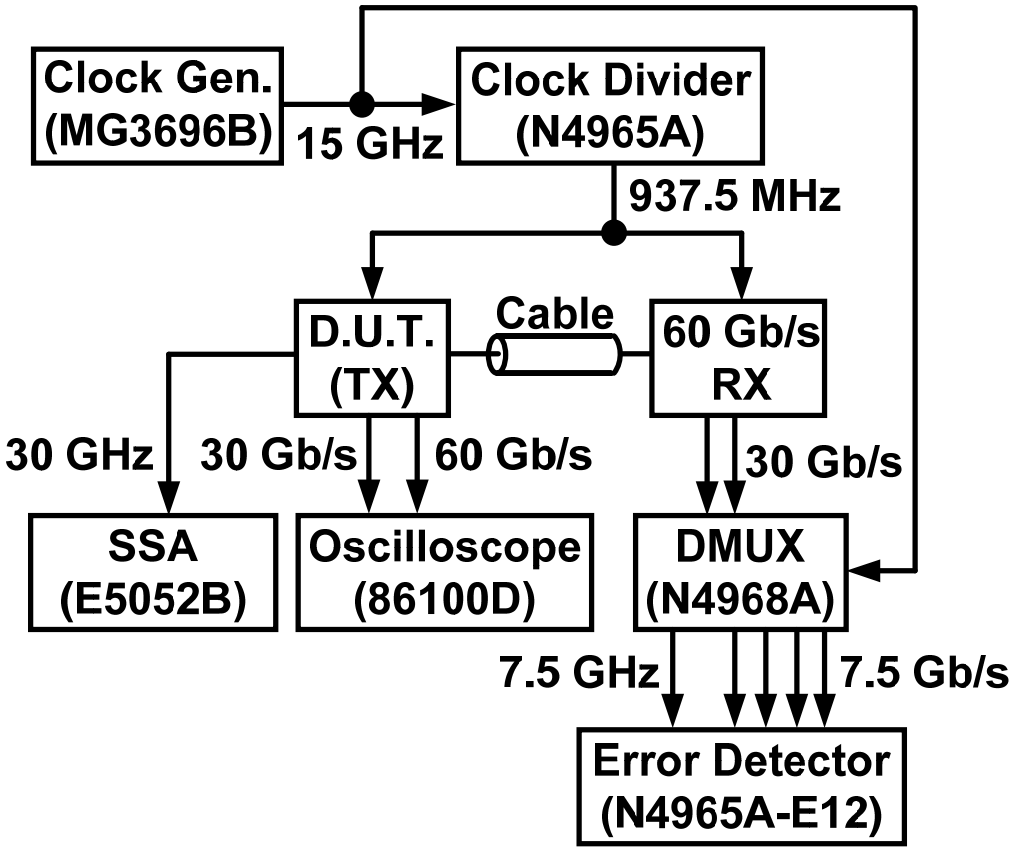


Level Spacing = 50mV
Horizontal Opening = 0.60UI
Vertical: 50mV/div
Horizontal: 10ps/div

- Pre-distortion compensates for nonlinear lasers

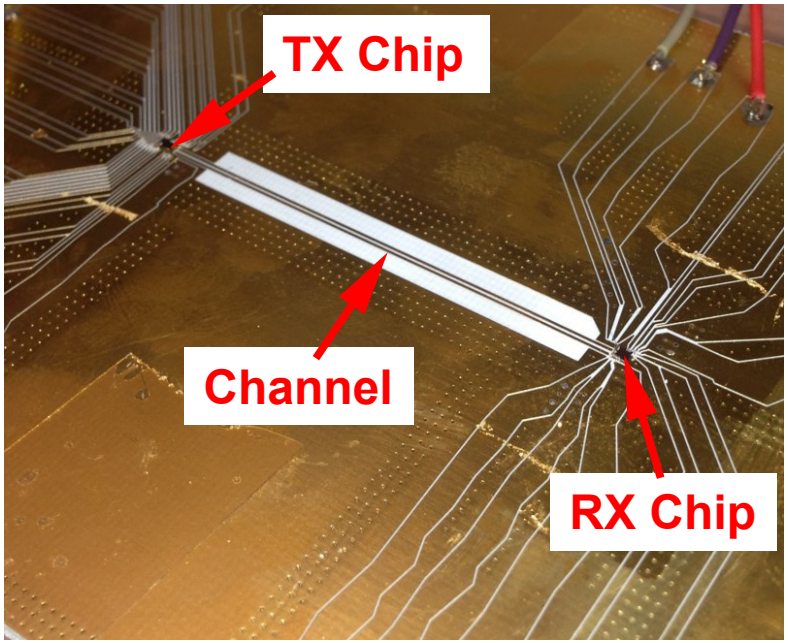
BER Testing Setup

NRZ TX



	Cable	Probe	Oscilloscope
Loss (dB)	–3.7@30GHz –5.5@60GHz	–0.9@30GHz –1.2@60GHz	–1.4@50GHz

PAM4 TX



- RX with 1:2 DMUX
- 5cm RO4003 channel
- $2^{31}-1$ PRBS, BER < 10^{-12}

Performance Summary

NRZ TX			
	[Yamazaki '04]	[Kanda '09]	This Work
Data Rate	50Gb/s	40Gb/s	60Gb/s
Function	2:1 MUX Only	SFI 5.2 Receiver + 4:1 MUX (40Gb/s) + 4:2 MUX (20Gb/s) + 20GHz PLL	4:1 MUX + 60GHz PLL + Built-in PRBS
TX Clock PNoise @ 1MHz	N/A	N/A	–100dBc/Hz
TX Clock RMS Jitter	N/A	N/A	461fs (1kHz~20MHz)
Data Input Range (S.E.)	$1V_{PP}$	N/A	$50\sim300mV_{PP}$
Clock Input Range (S.E.)	$1V_{PP}$	N/A	$100\sim300mV_{PP}$
Data Swing (S.E.) Full-Rate Half-Rate	$70mV_{PP}$ (50Gb/s) N/A	$325mV_{PP}$ (40Gb/s) $400mV_{PP}$ (20Gb/s)	$250mV_{PP}$ (60Gb/s) $250mV_{PP}$ (30Gb/s)
Data Jitter	N/A	783fs,rms (40Gb/s)	1.08ps,rms (30Gb/s)*
20-80% Rise/Fall Time Full Rate Half-Rate	10.4ps (50Gb/s) N/A	10.22ps (40Gb/s) 14.67ps (20Gb/s)	8.0ps (60Gb/s) 7.5ps (30Gb/s)
Power Consumption	43mW	1.8W (40Gb/s mode)	450mW (MUX: 31mW)
Chip Area	1.8 x 1mm^2	4.2 x 4.2mm^2	2.1 x 1mm^2
Technology	90nm CMOS (Shrunk to 48nm)	65nm Digital CMOS	65nm Digital CMOS

PAM4 TX		
	[Menolfi '05]	This Work
Data Rate	25Gb/s	60Gb/s
Function	Combiner + FFE	Combiner + FFE + Built-in PLL
TX Clock PNoise @ 1MHz	N/A	–98.5dBc/Hz
TX Clock RMS Jitter	N/A	508fs (100Hz~1GHz)
Data Input Range (S.E.)	N/A	$50\sim300mV_{PP}$
Clock Input Range (S.E.)	N/A	$100\sim300mV_{PP}$
D_{OUT} Full Mag. (4 Levels)	$430mV_{PP}$	$250mV_{PP}$
Min. Eye Opening	$90mV_{PP}$	$50mV_{PP}$
Horizontal Eye Opening	>0.4UI @ 25Gb/s	>0.6UI @ 60Gb/s
20-80% Rise/Fall Time	29ps @ 25Gb/s	12.8ps @ 60Gb/s
Power Consumption	101.8mW	290mW
Chip Area	1 x 0.5mm^2	1.2 x 0.95mm^2
Technology	90nm SOI CMOS	65nm Digital CMOS

* For half-rate D_{OUT}. Full-rate data jitter is not measurable due to the limited bandwidth of oscilloscope.

Conclusions

- Broadband circuit techniques and EM skills help further boosting data rate and performance.
- Built-in PLL increases TX design robustness.
- Board-level co-design become essential as data rate goes up to 50+Gb/s.
- First NRZ and PAM4 transmitters operating at 60Gb/s have been realized in CMOS.

Paper 2.4

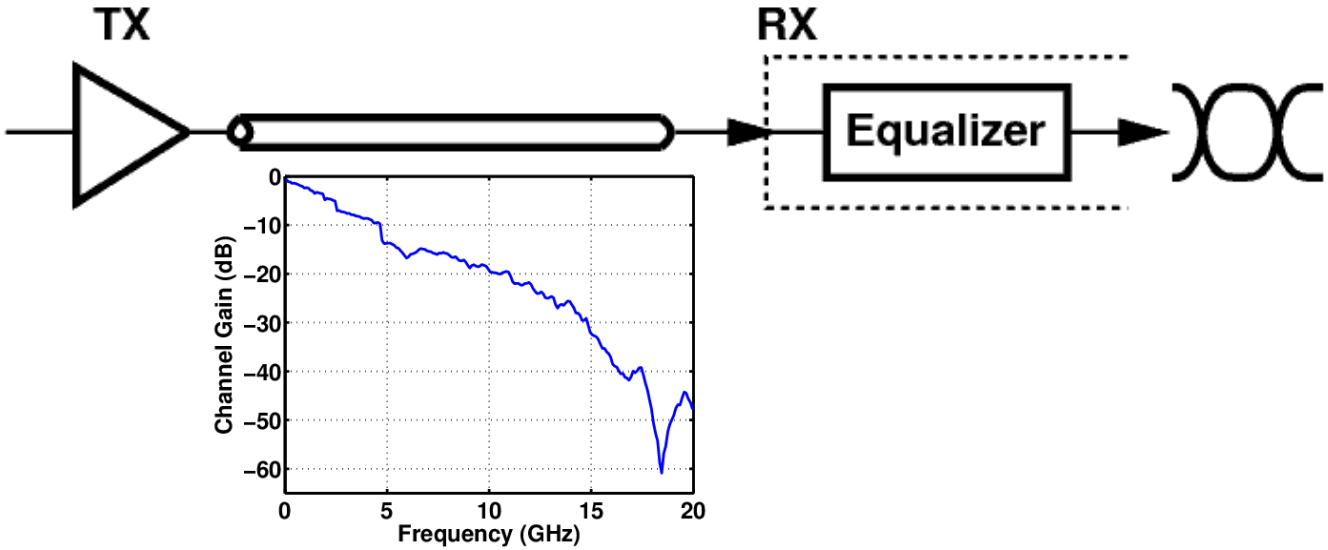
A 25Gb/s 5.8mW CMOS Equalizer

Jun Won Jung and Behzad Razavi
Electrical Engineering Department
University of California, Los Angeles

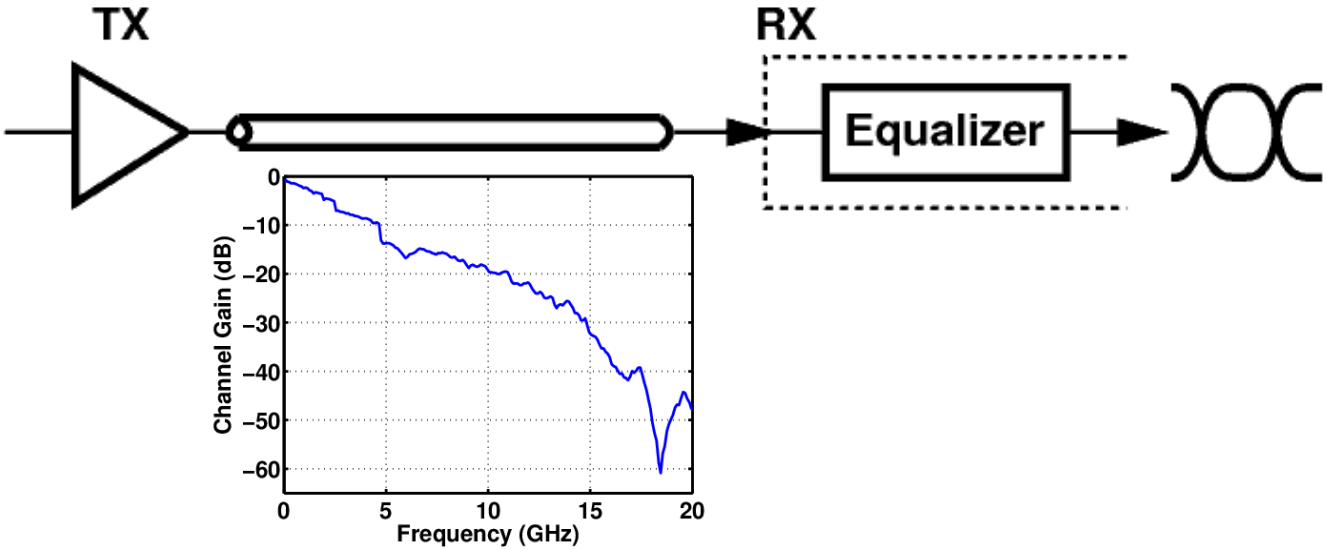
Outline

- Introduction
- Charge Steering
- DFE Architectures
- Evolution of Proposed Architecture
- Building Blocks
- Experimental Results
- Conclusion

Introduction



Introduction

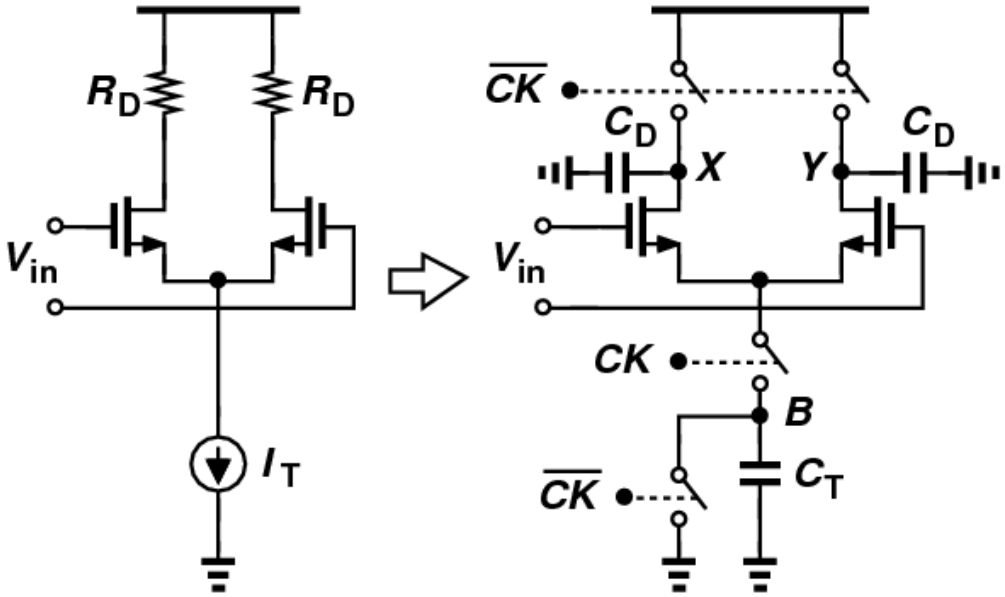


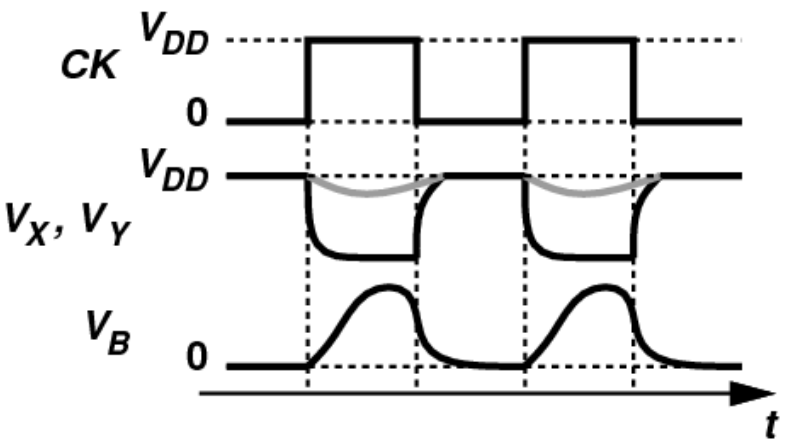
- **Energy per bit does not tell the entire story:**

Reference	A. Agrawal ISSCC 2012	J. Bulzacchelli ISSCC 2012	K. Jung ISSCC 2013	K. Kaviani CICC 2012	J. E. Proesel VLSI 2011
Data Rate	19 Gb/s	28 Gb/s	22 Gb/s	27 Gb/s	20 Gb/s
Channel Loss @ Nyquist	25 dB	35 dB	16 dB	>10 dB	26.3 dB
BER / Horizontal Eye Opening	$< 10^{-9}$ / 36 % UI	$< 10^{-9}$ / 35.6 % UI	$< 10^{-12}$ / 26 % UI	$< 10^{-9}$ / 26 % UI	$< 10^{-8}$ / 26 % UI
Power (mW)	118	80 *	20.6	11.1	13.2

*Only for odd and even DFEs. Excludes CTLE, etc.

Charge Steering

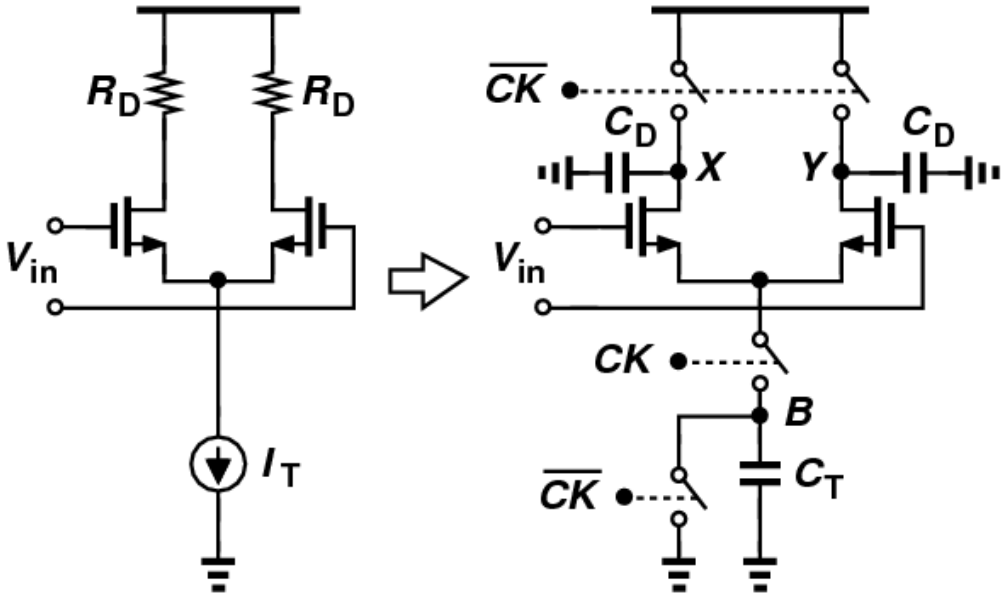


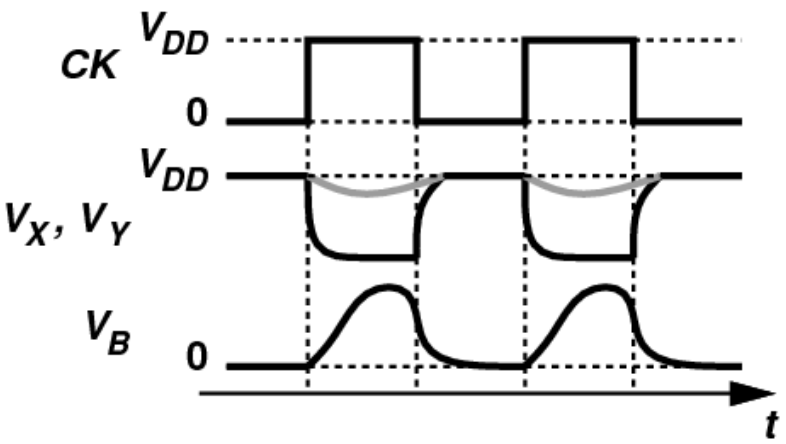


[Jung&Razavi, JSSC, March 13]

- No static power
- Moderate differential swings
  - Fast
  - Better supply rejection than single-ended rail-to-rail logic

Charge Steering

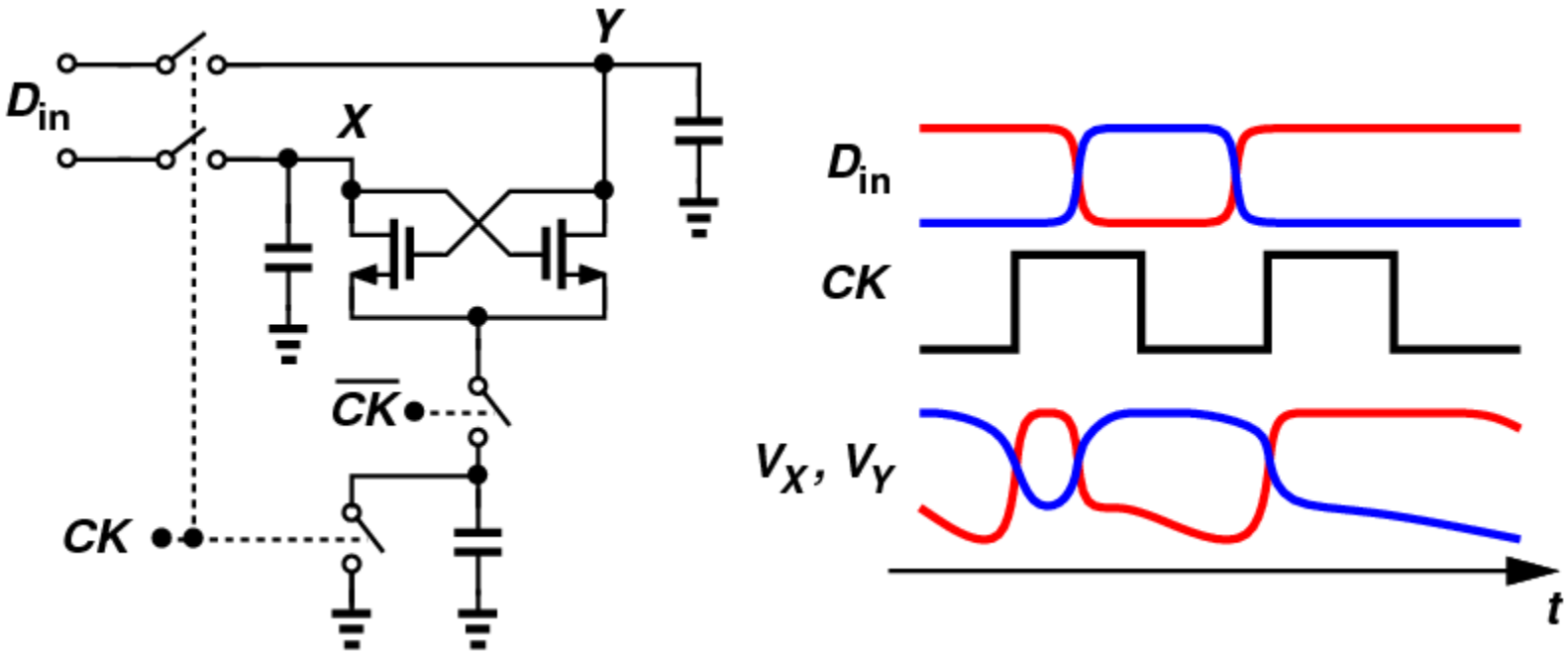




[Jung&Razavi, JSSC, March 13]

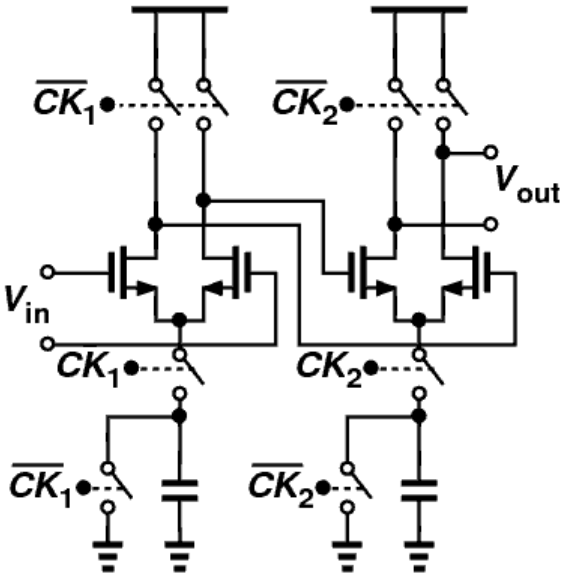
- No static power
- Moderate differential swings
  - Fast
  - Better supply rejection than single-ended rail-to-rail logic
- Output in RZ form

NRZ Charge-Steering Latch?



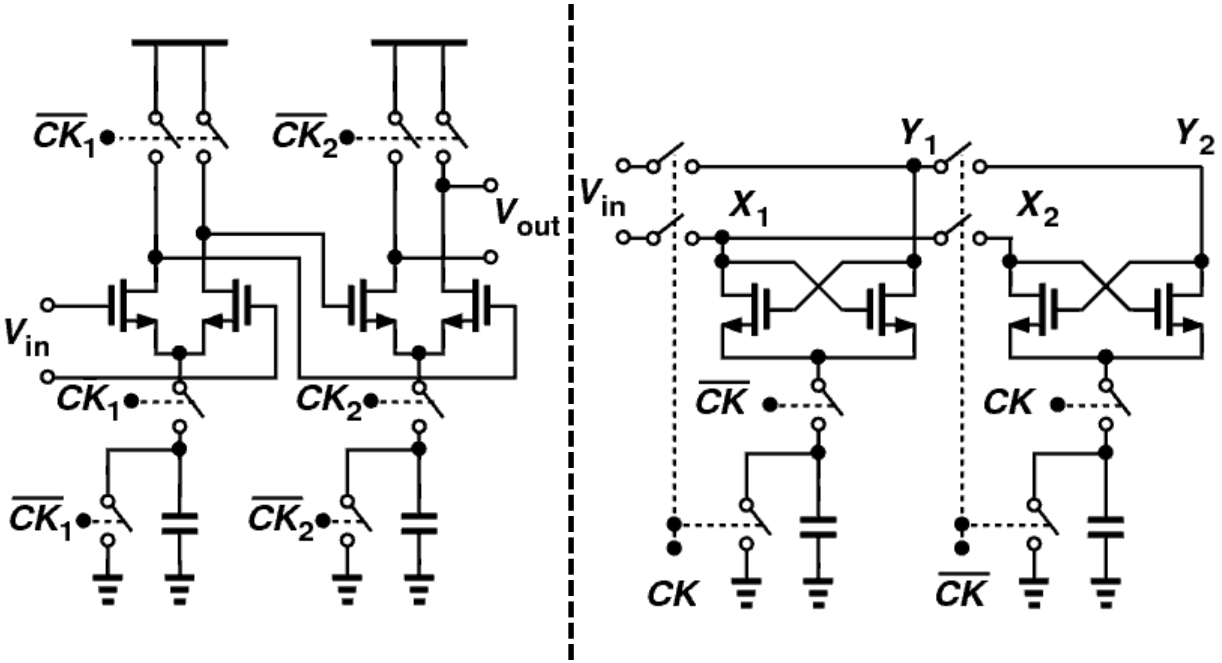
- Merges sampling and reset modes.

Cascading Issues



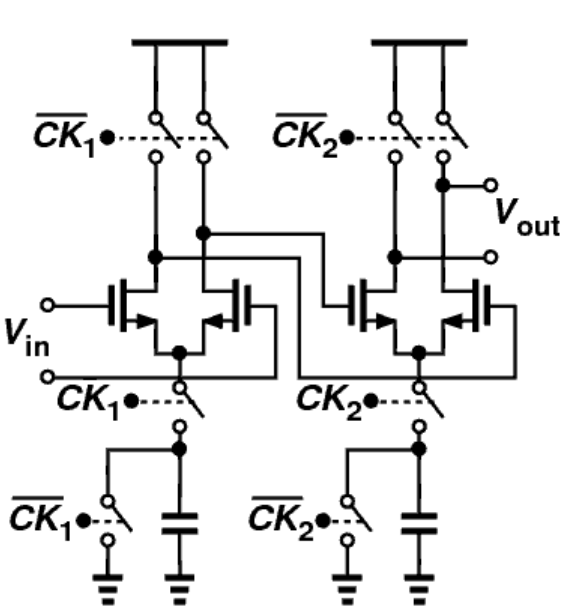
- **Requires quadrature clocks**

Cascading Issues

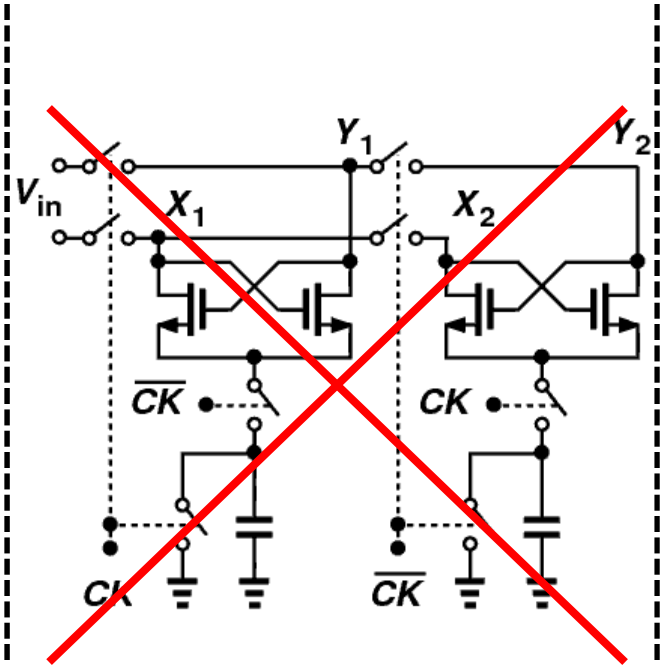


- Requires quadrature clocks
- Severe charge sharing

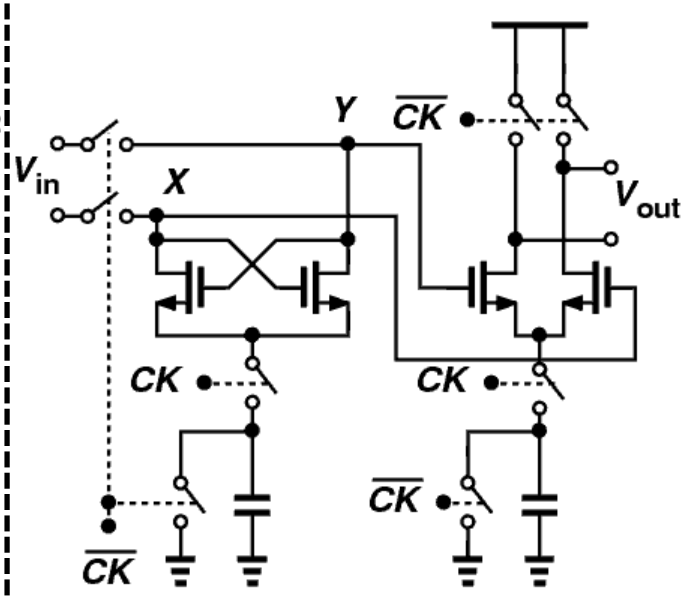
Cascading Issues



- Requires quadrature clocks

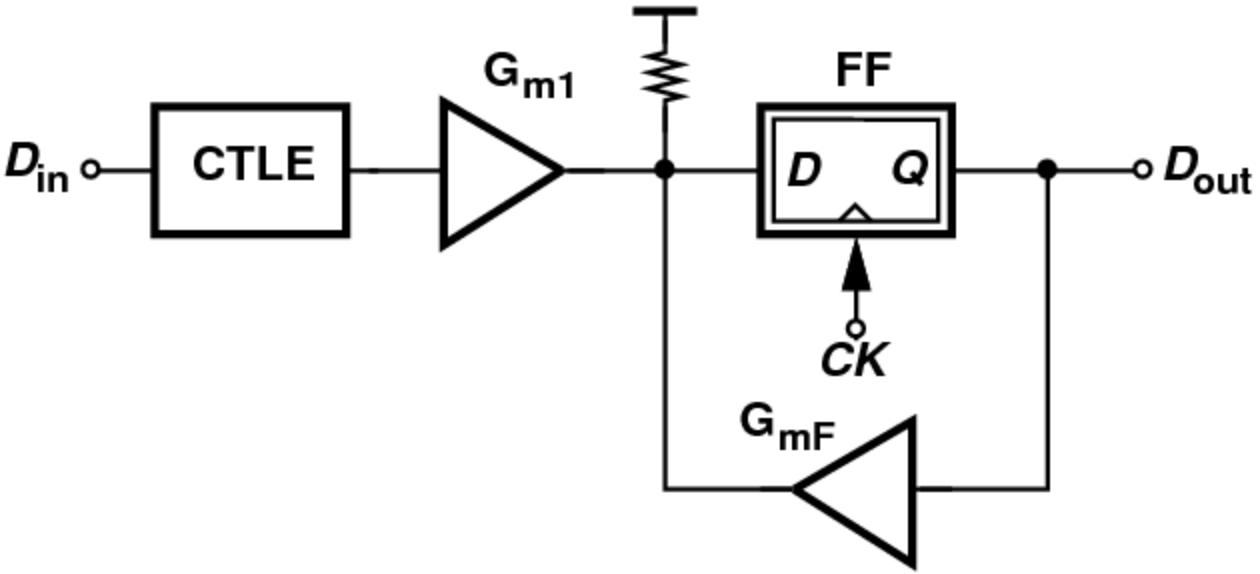


- Severe charge sharing



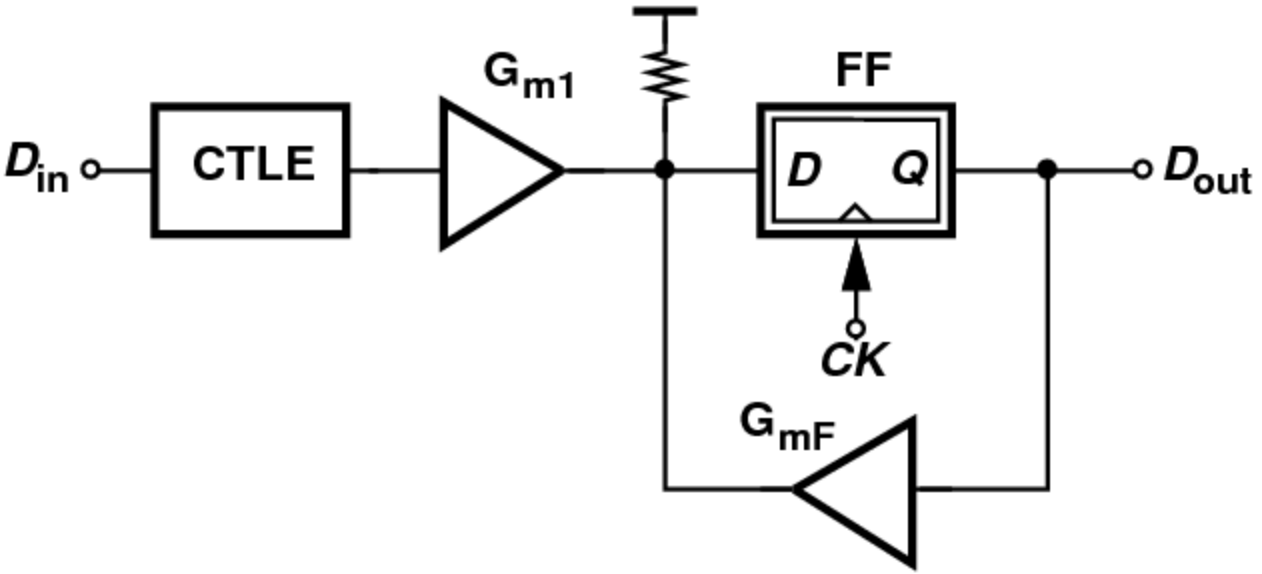
- No race conditions

Equalizer Design Considerations



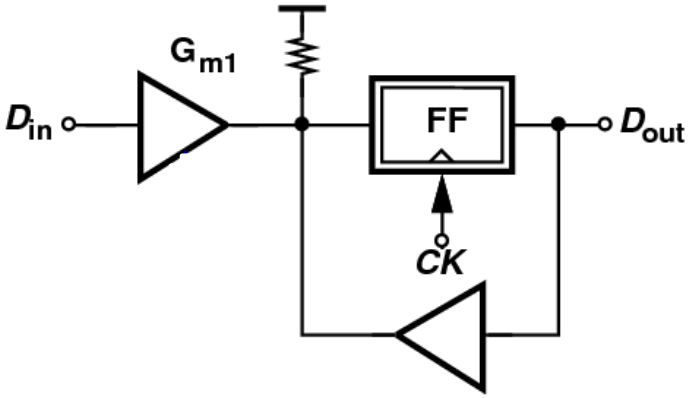
- Direct DFE vs. Loop Unrolling
- Full Rate vs. Half Rate vs. Quarter Rate
  - Clock generation and distribution
  - Load seen by CTLE

Equalizer Design Considerations



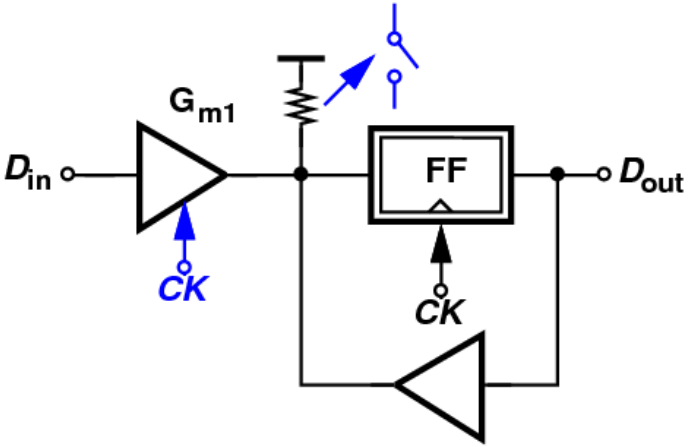
- Direct DFE vs. Loop Unrolling
- Full Rate vs. Half Rate vs. Quarter Rate
  - Clock generation and distribution
  - Load seen by CTLE
- How to deal with RZ waveforms?
- Can we use a charge-steering summer?

To Reset or Not to Reset



$$t_{cq} + t_{setup} + t_{FB} < 1 \text{ UI}$$

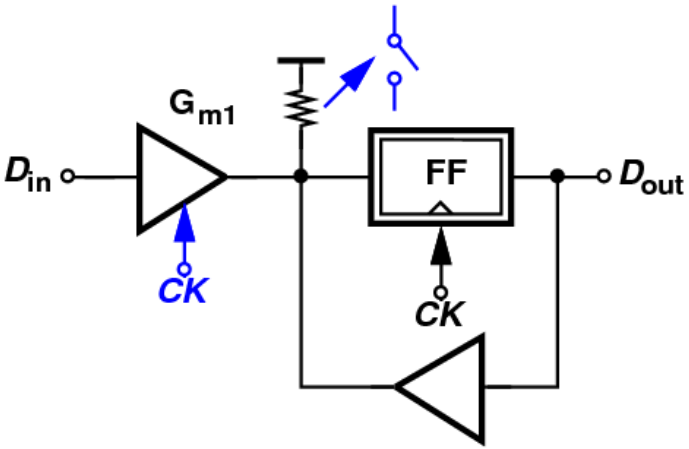
To Reset or Not to Reset



$$t_{cq} + t_{setup} + t_{FB} < 1 \text{ UI}$$

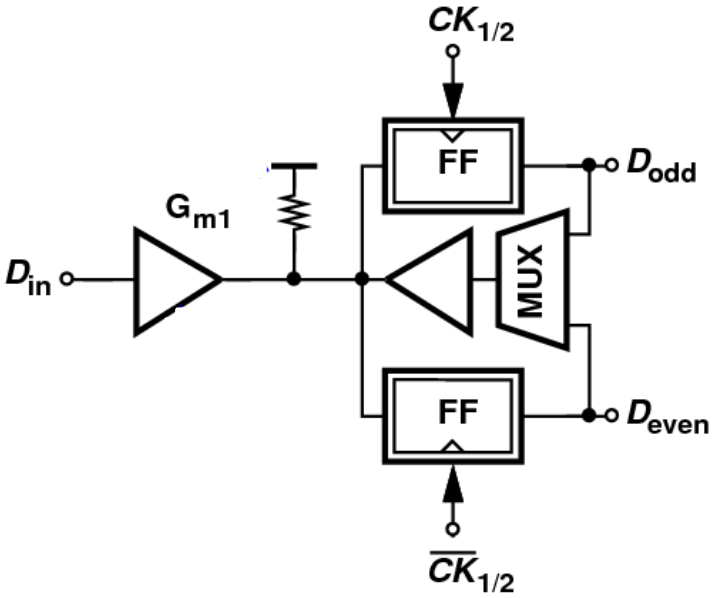
$$t_{cq} + t_{setup} < \frac{1}{2} \text{ UI}$$

To Reset or Not to Reset



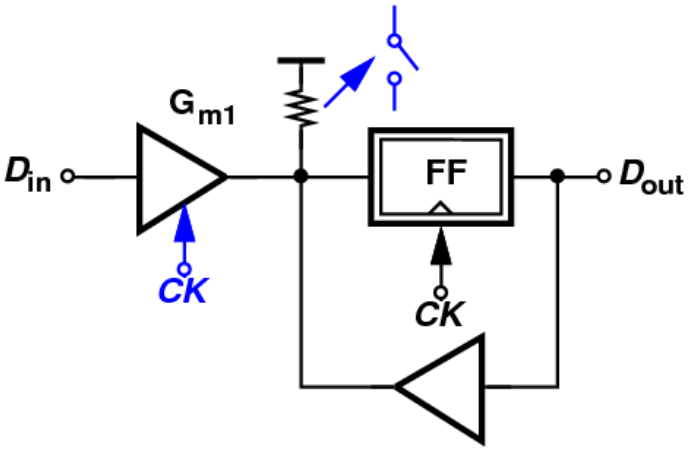
$$t_{cq} + t_{setup} + t_{FB} < 1 \text{ UI}$$

$$t_{cq} + t_{setup} < \tfrac{1}{2} \text{ UI}$$



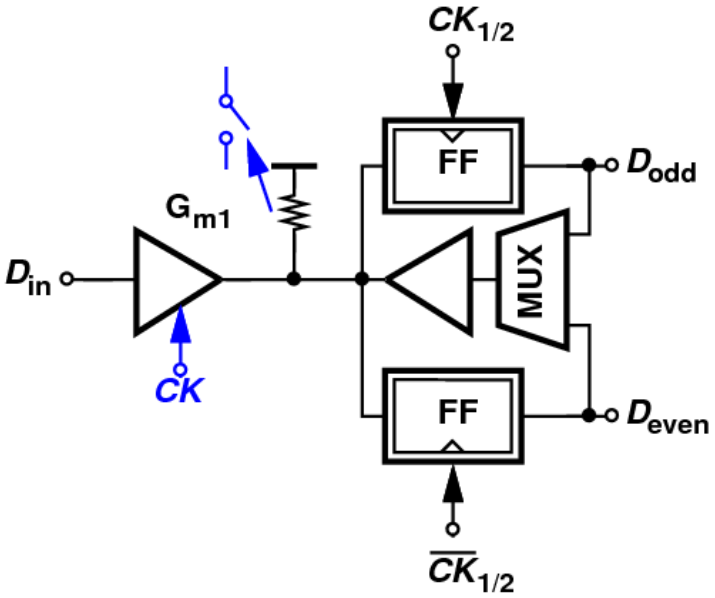
$$t_{cq} + t_{setup} + t_{MUX} + t_{FB} < 1 \text{ UI}$$

To Reset or Not to Reset



$$t_{cq} + t_{setup} + t_{FB} < 1 \text{ UI}$$

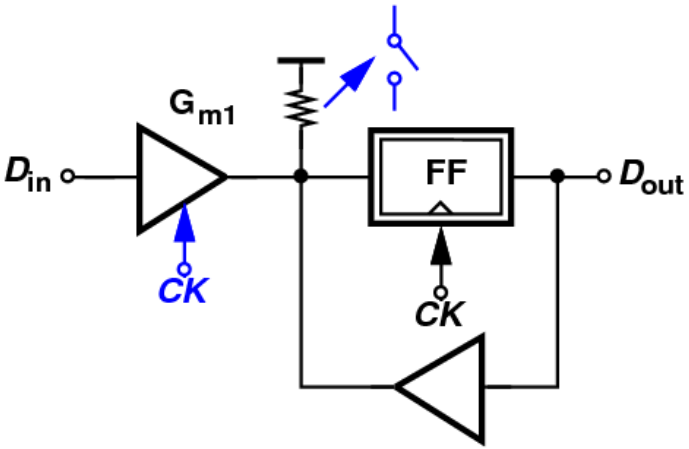
$$t_{cq} + t_{setup} < \frac{1}{2} \text{ UI}$$



$$t_{cq} + t_{setup} + t_{MUX} + t_{FB} < 1 \text{ UI}$$

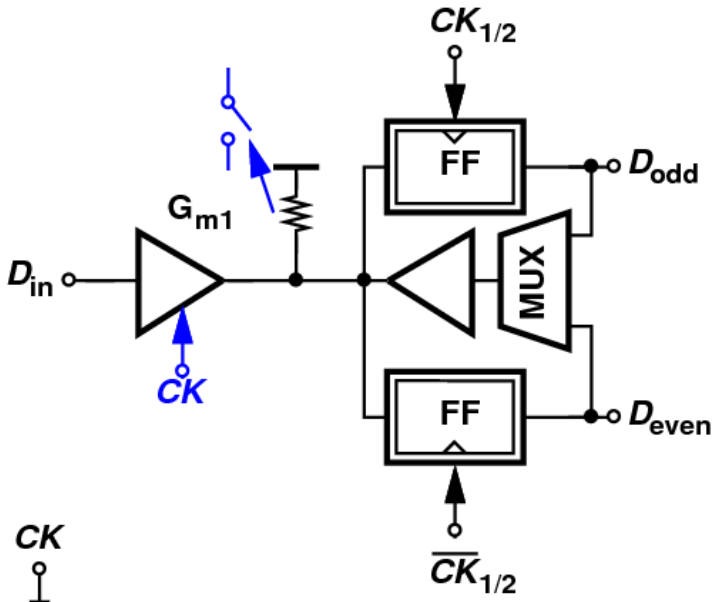
$$t_{cq} + t_{setup} + t_{MUX} < \frac{1}{2} \text{ UI}$$

To Reset or Not to Reset



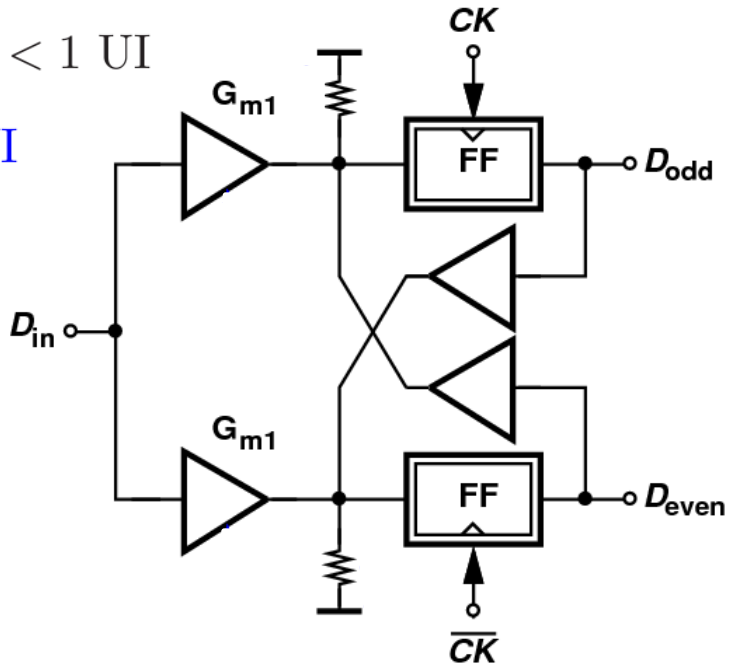
$$t_{cq} + t_{setup} + t_{FB} < 1 \text{ UI}$$

$$t_{cq} + t_{setup} < \tfrac{1}{2} \text{ UI}$$



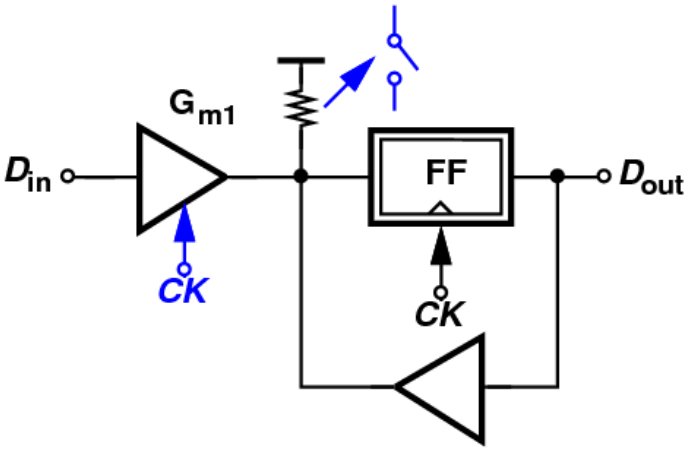
$$t_{cq} + t_{setup} + t_{MUX} + t_{FB} < 1 \text{ UI}$$

$$t_{cq} + t_{setup} + t_{MUX} < \tfrac{1}{2} \text{ UI}$$



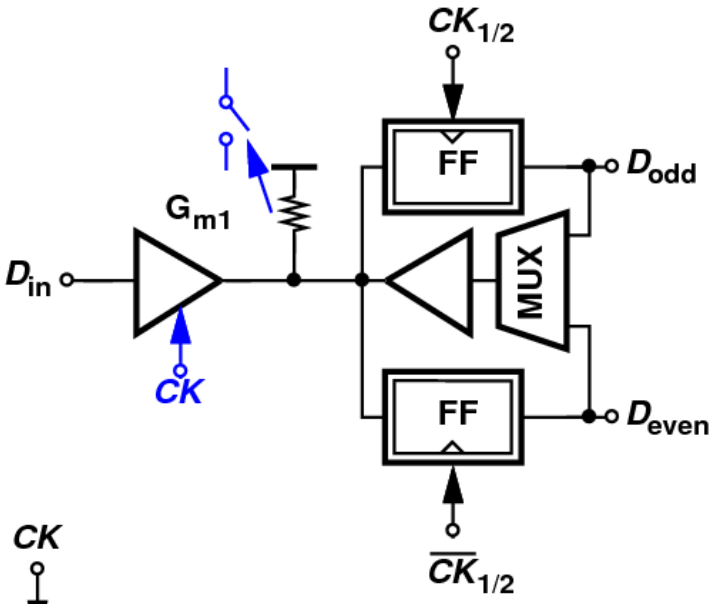
$$t_{cq} + t_{setup} + t_{FB} < 1 \text{ UI}$$

To Reset or Not to Reset



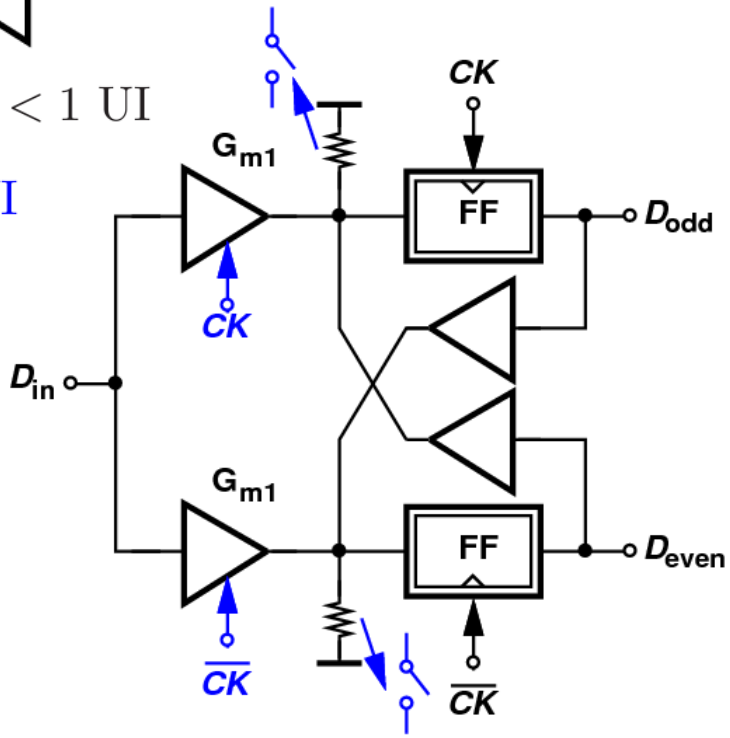
$$t_{cq} + t_{setup} + t_{FB} < 1 \text{ UI}$$

$$t_{cq} + t_{setup} < \tfrac{1}{2} \text{ UI}$$



$$t_{cq} + t_{setup} + t_{MUX} + t_{FB} < 1 \text{ UI}$$

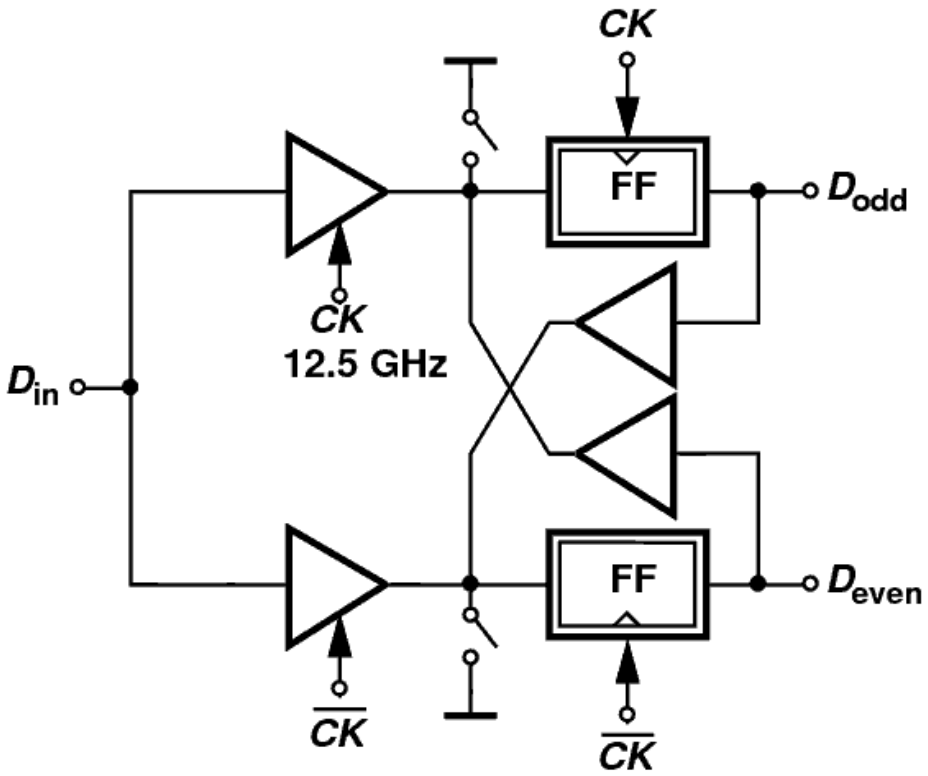
$$t_{cq} + t_{setup} + t_{MUX} < \tfrac{1}{2} \text{ UI}$$



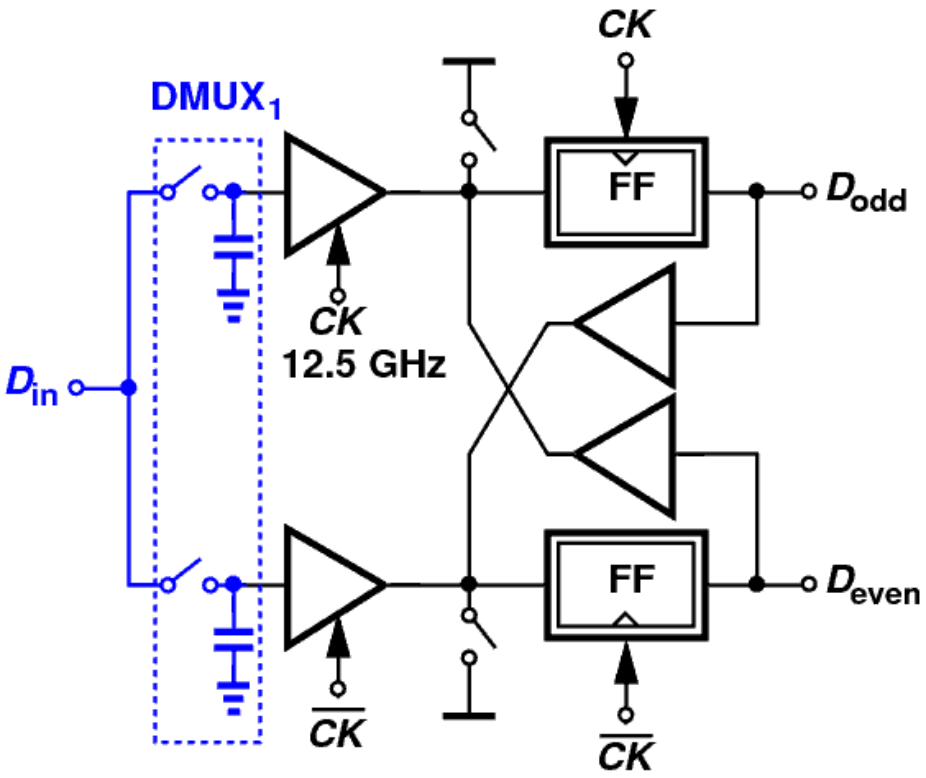
$$t_{cq} + t_{setup} + t_{FB} < 1 \text{ UI}$$

$$t_{cq} + t_{setup} < 1 \text{ UI}$$

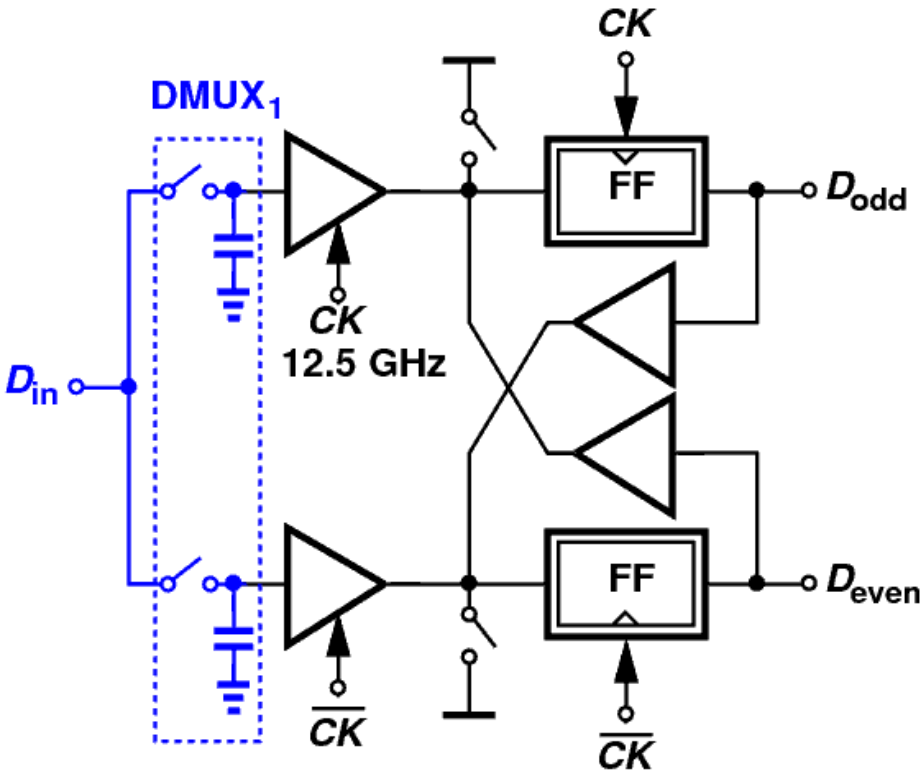
Half-Rate Charge-Steering DFE?

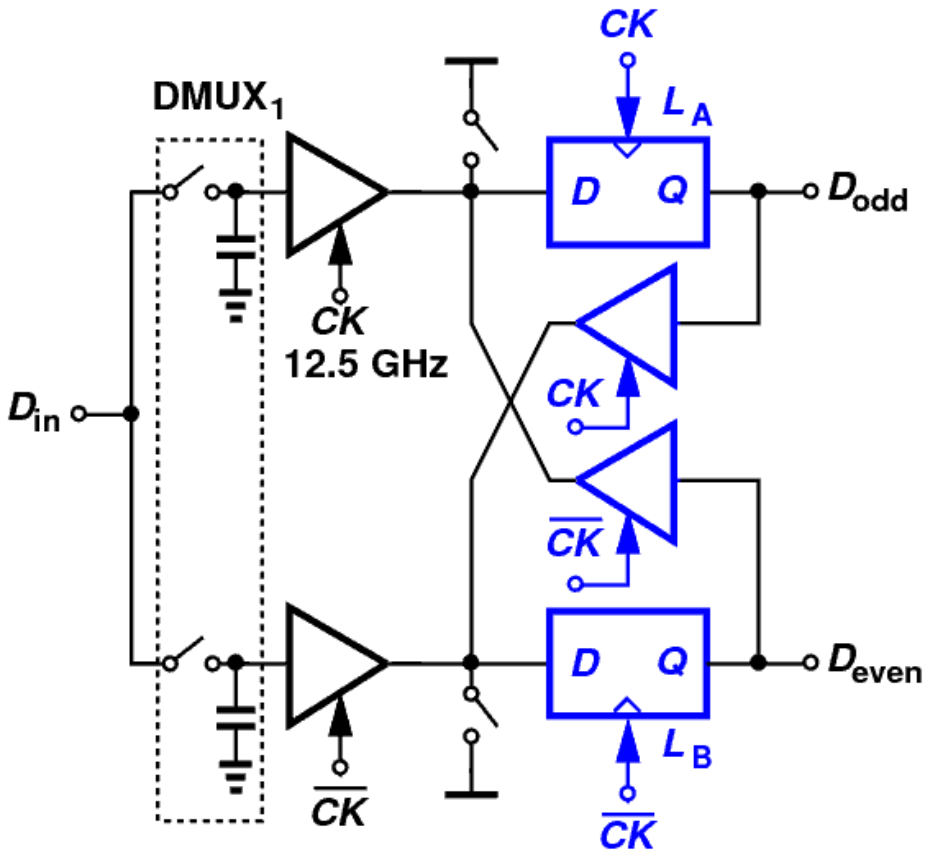


Half-Rate Charge-Steering DFE?

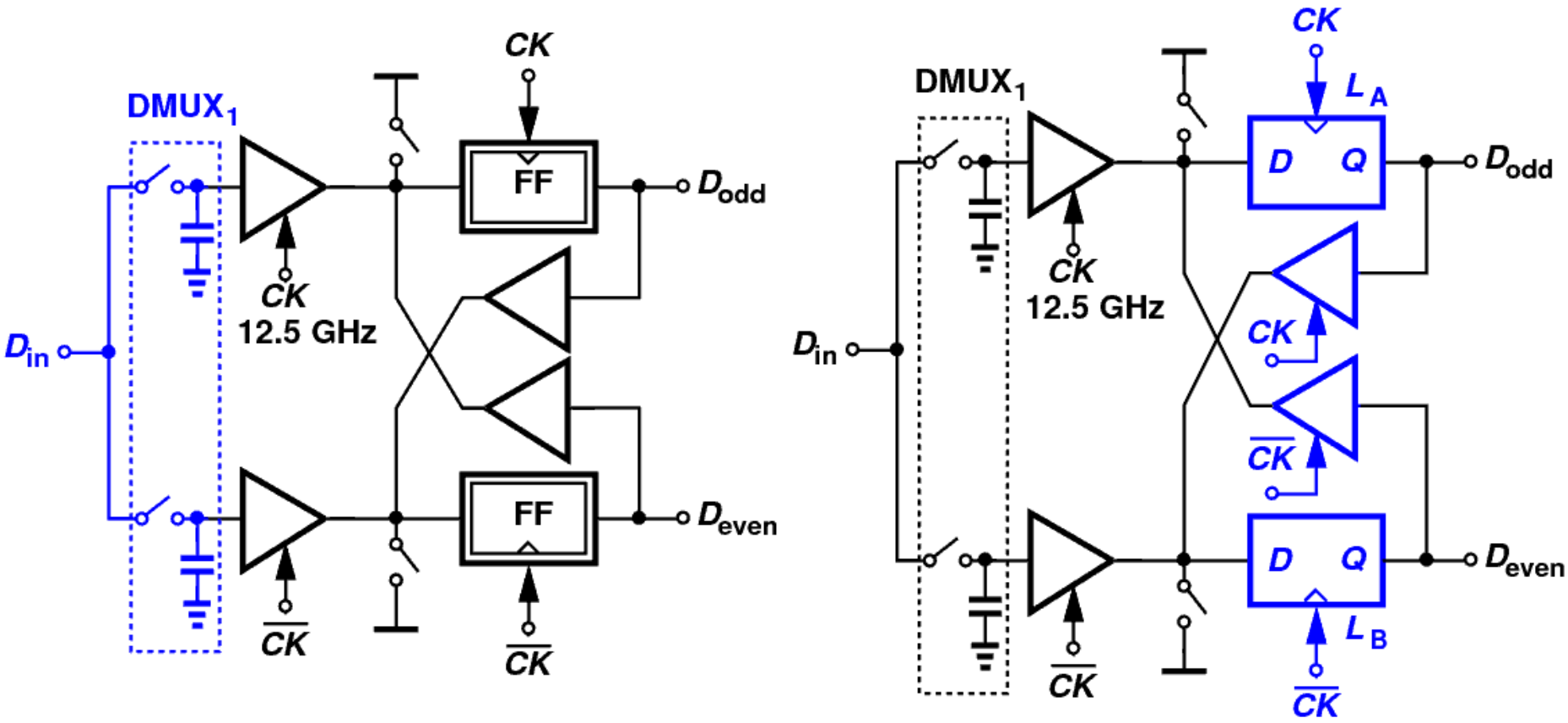


Half-Rate Charge-Steering DFE?



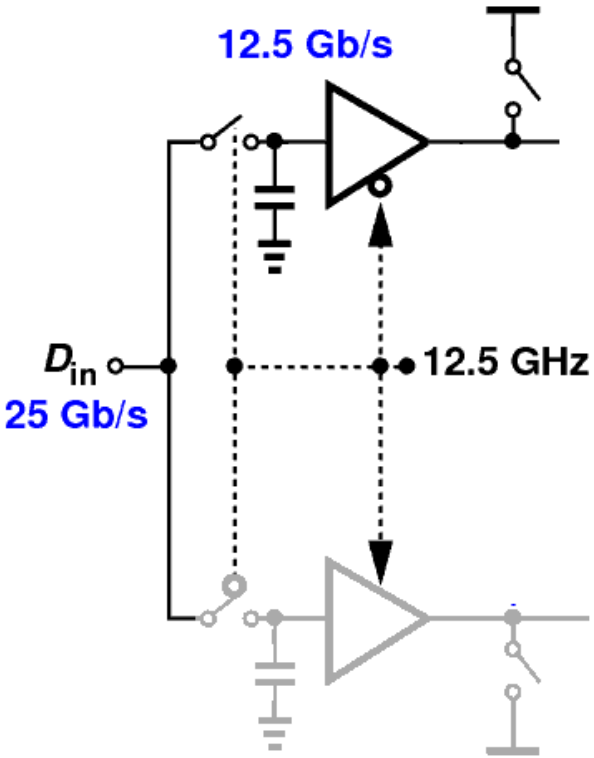


Half-Rate Charge-Steering DFE?

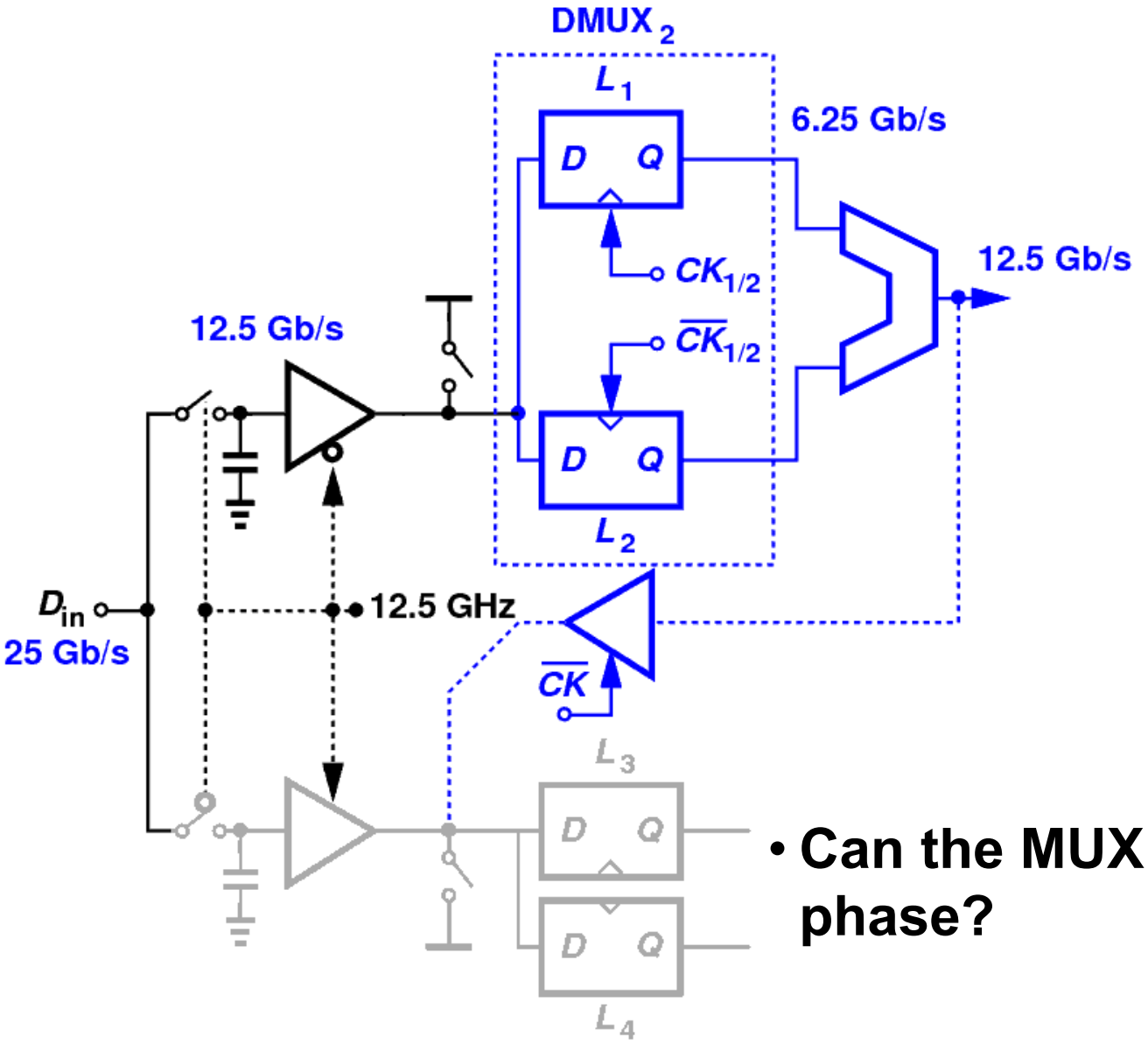


- Race condition between L_A (or L_B) and feedback Gm stage.

There's still hope …

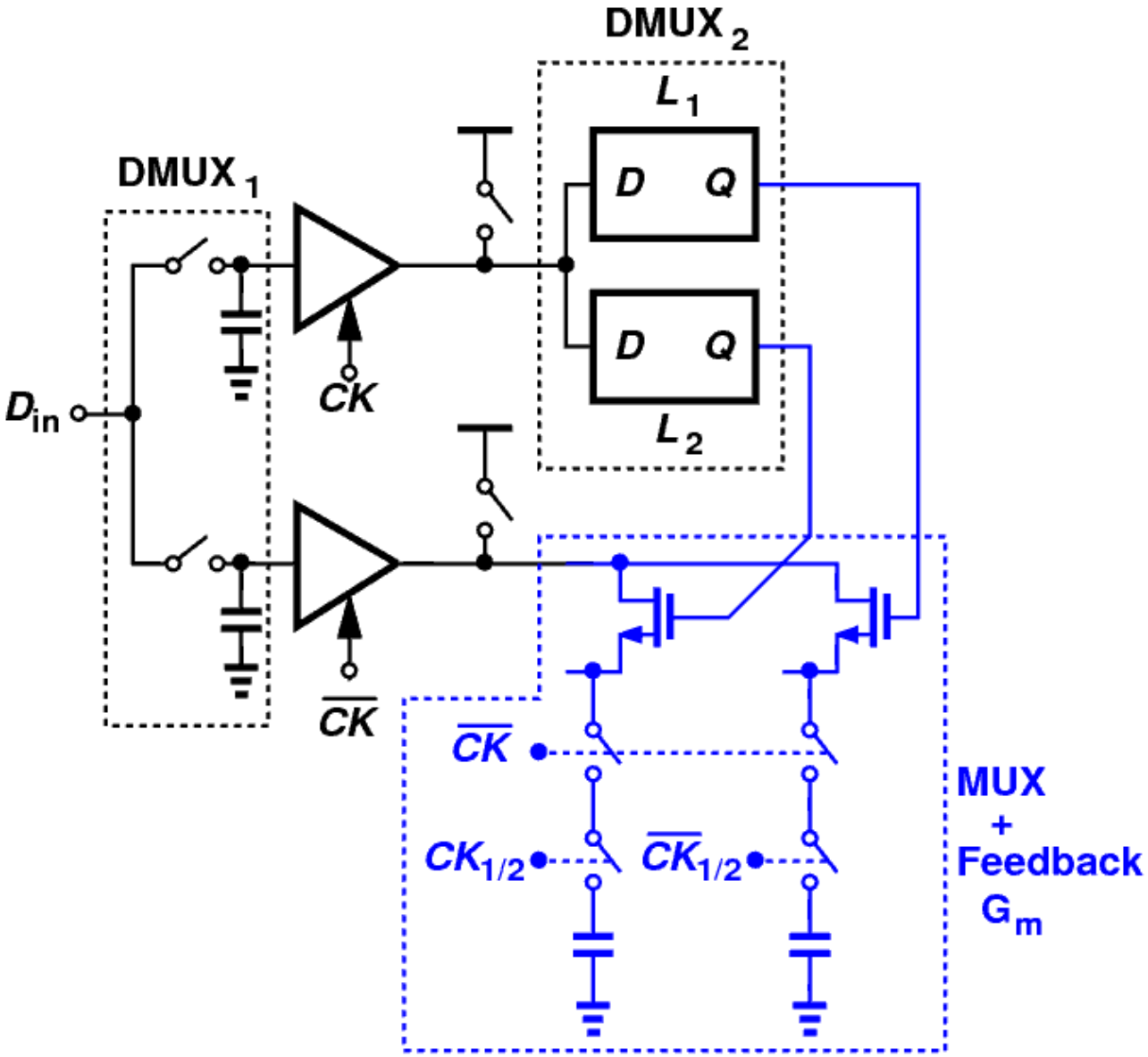


There's still hope …

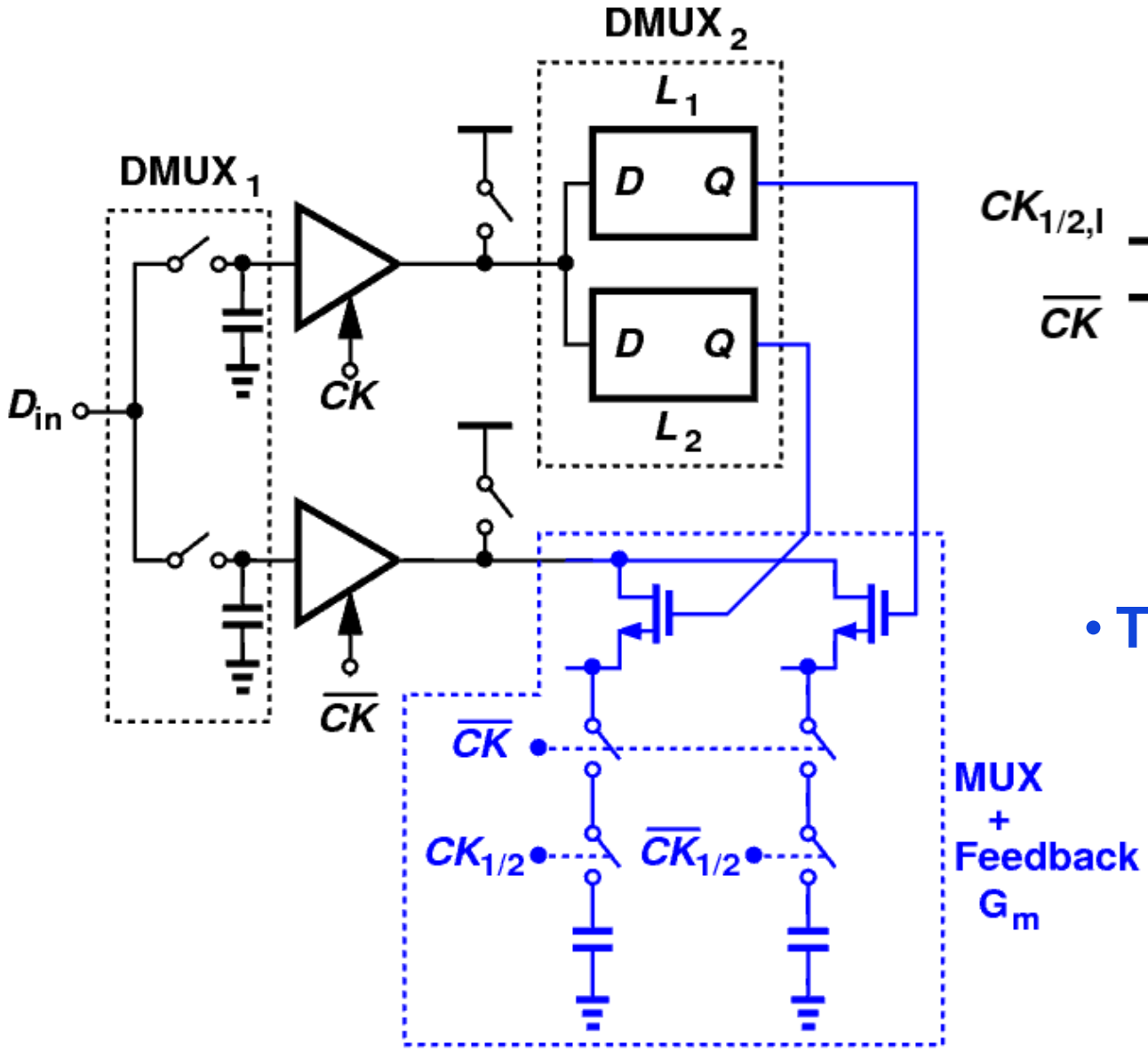


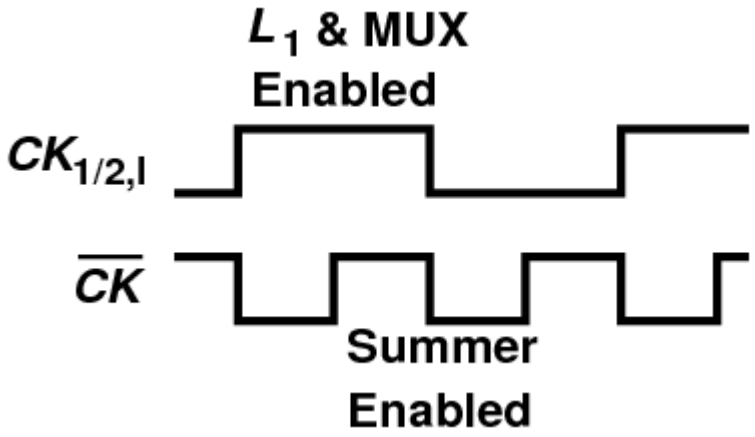
- Can the MUX avoid the reset phase?

Closing the Loop



Closing the Loop

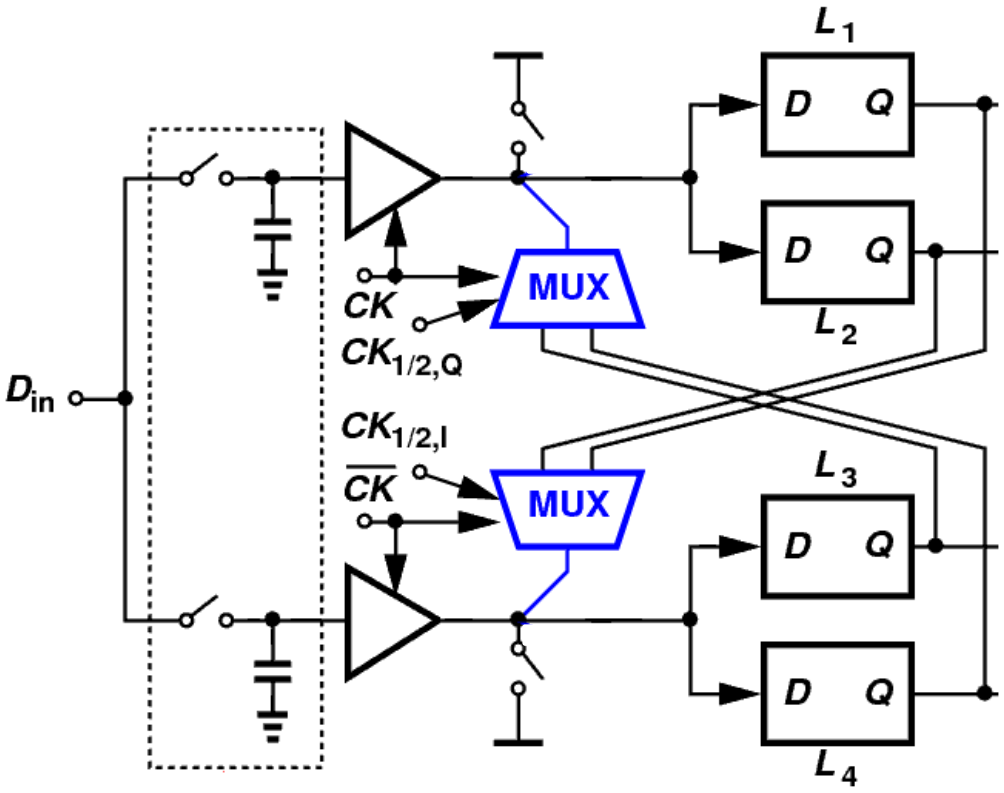




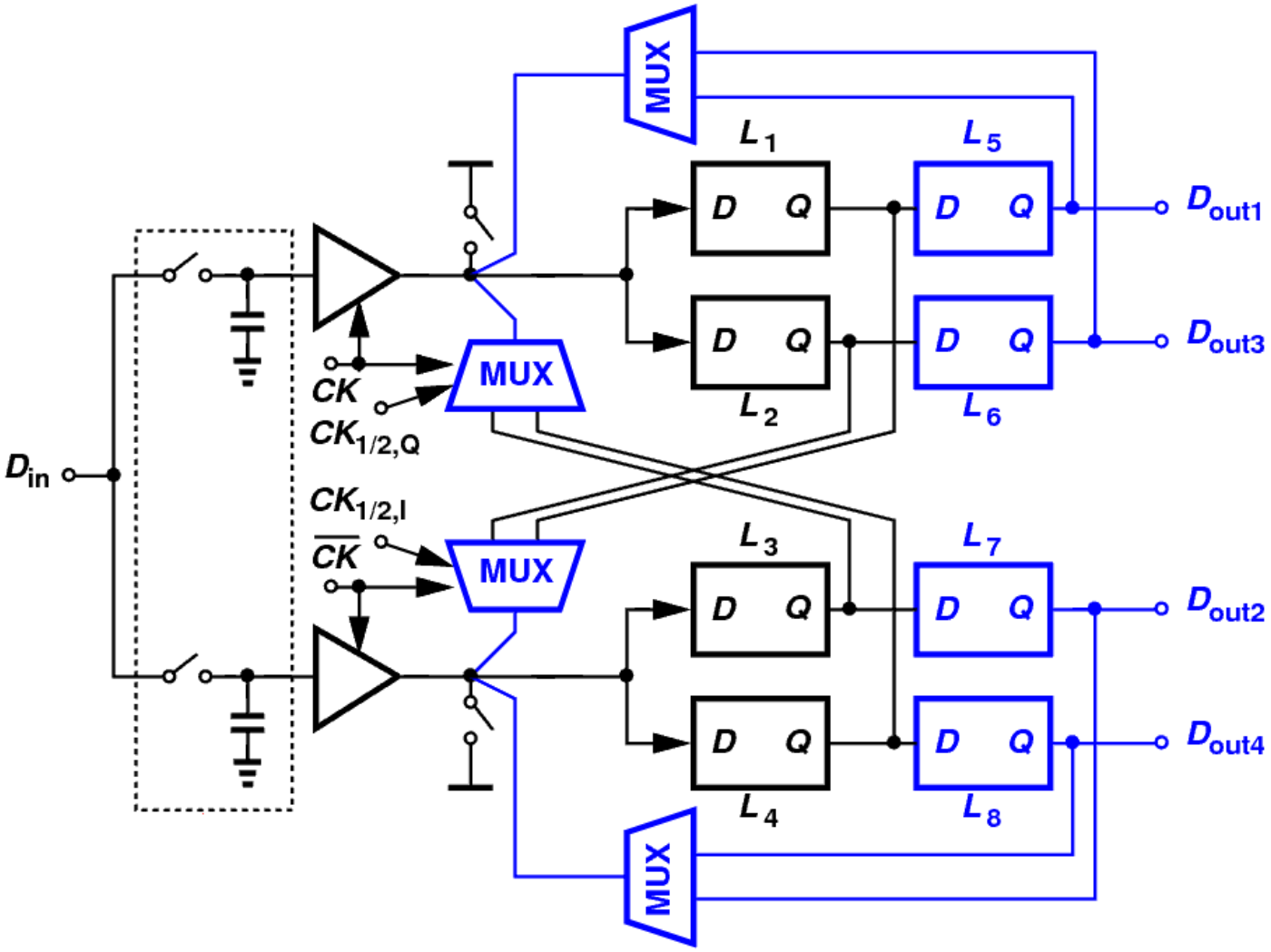
- **Timing Constraint :**

$$t_{cq} < 1 \text{ UI}$$

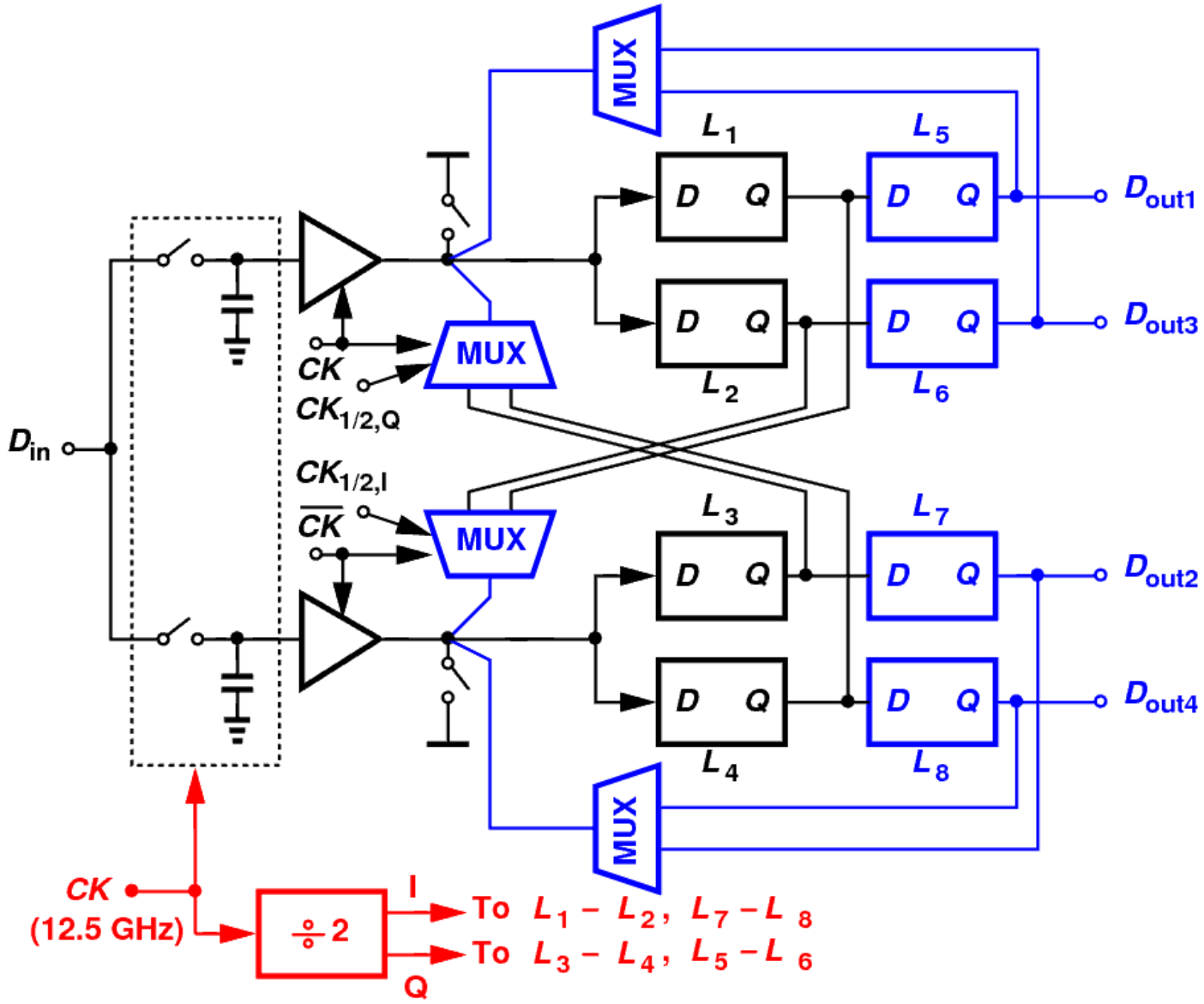
Addition of Second Tap



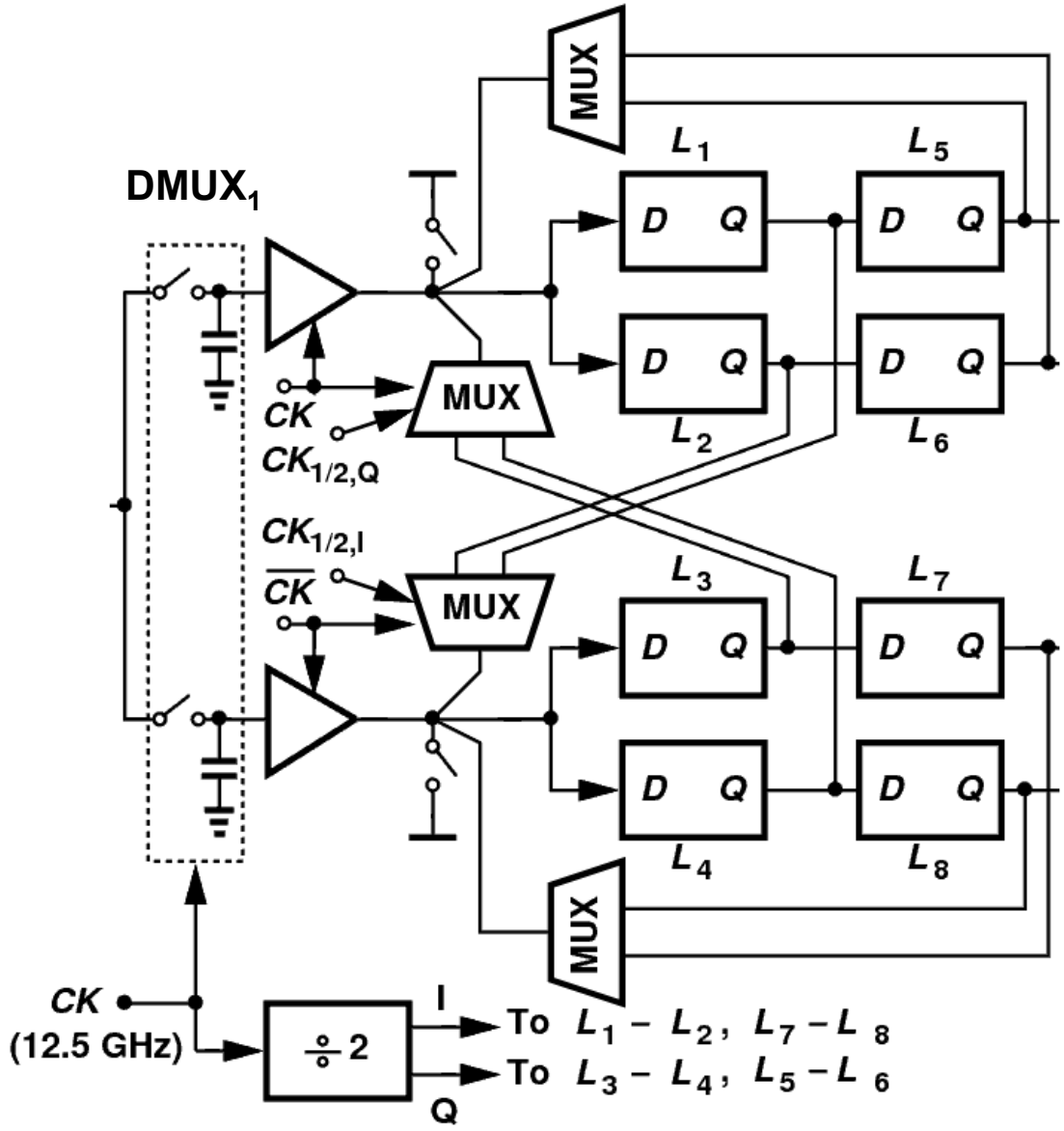
Addition of Second Tap



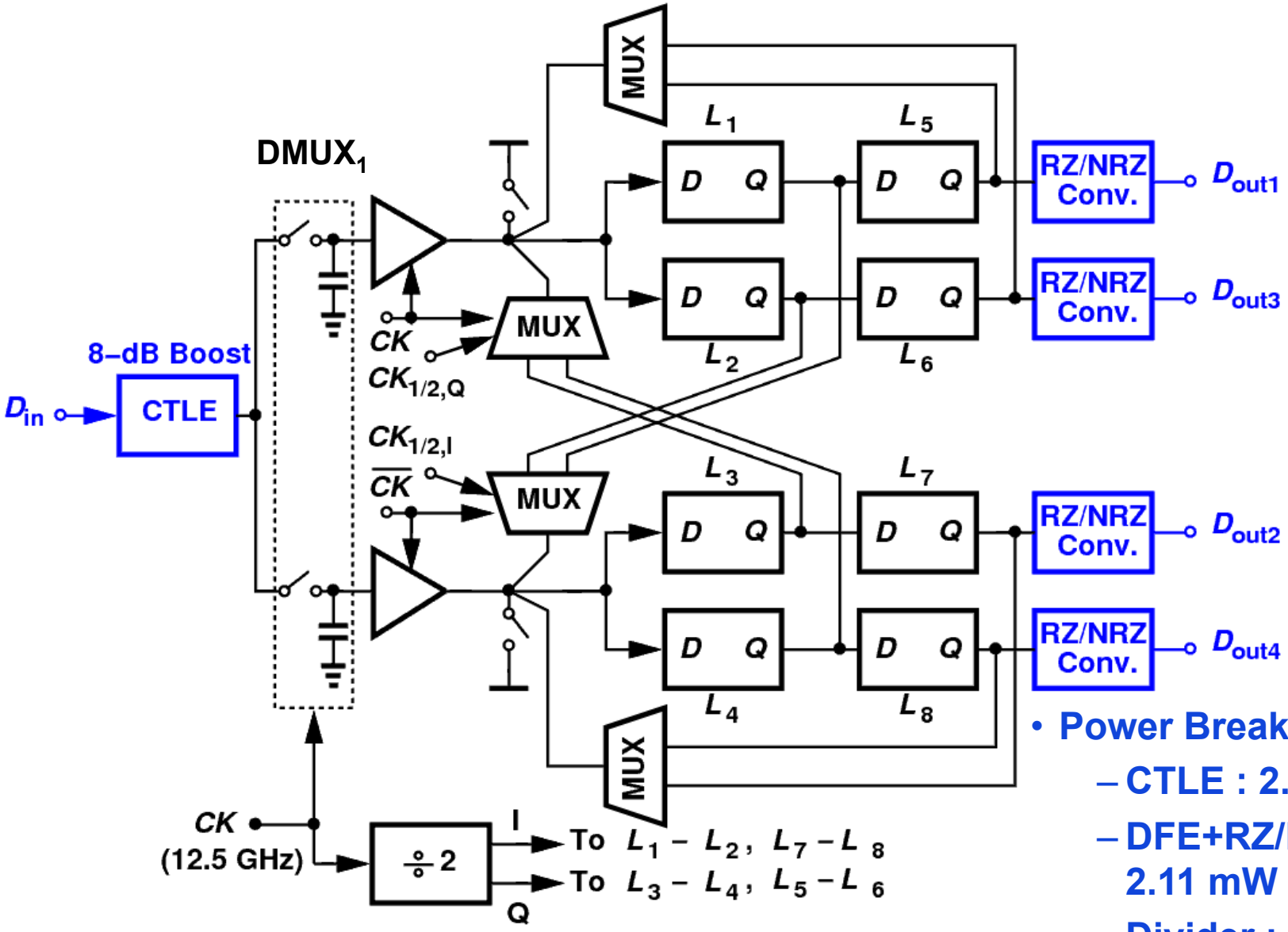
Addition of Second Tap



Complete Equalizer

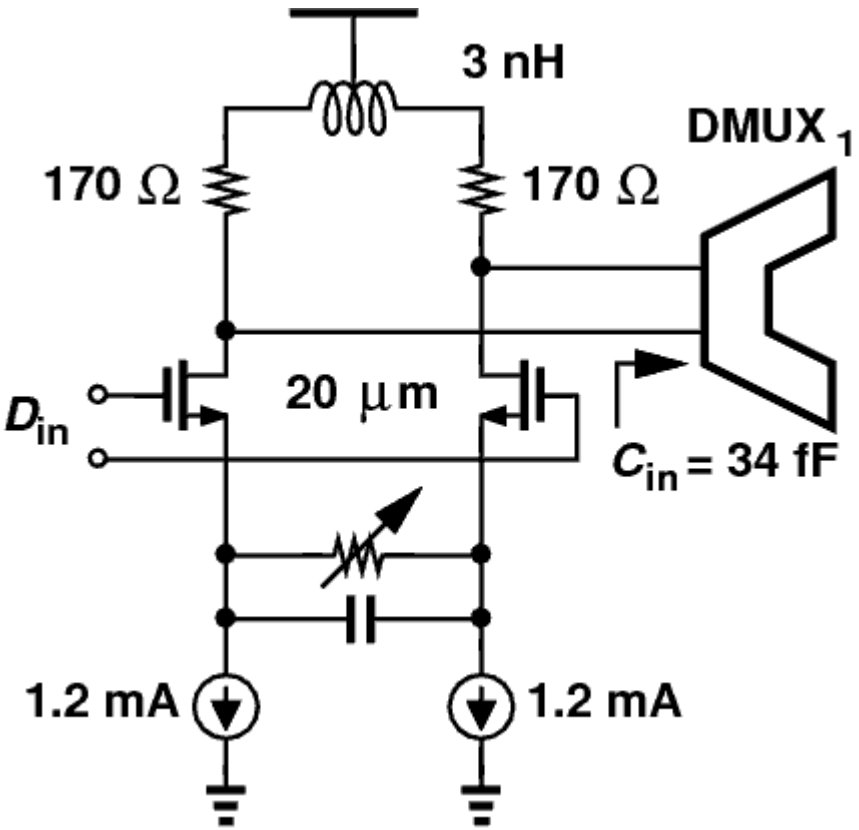


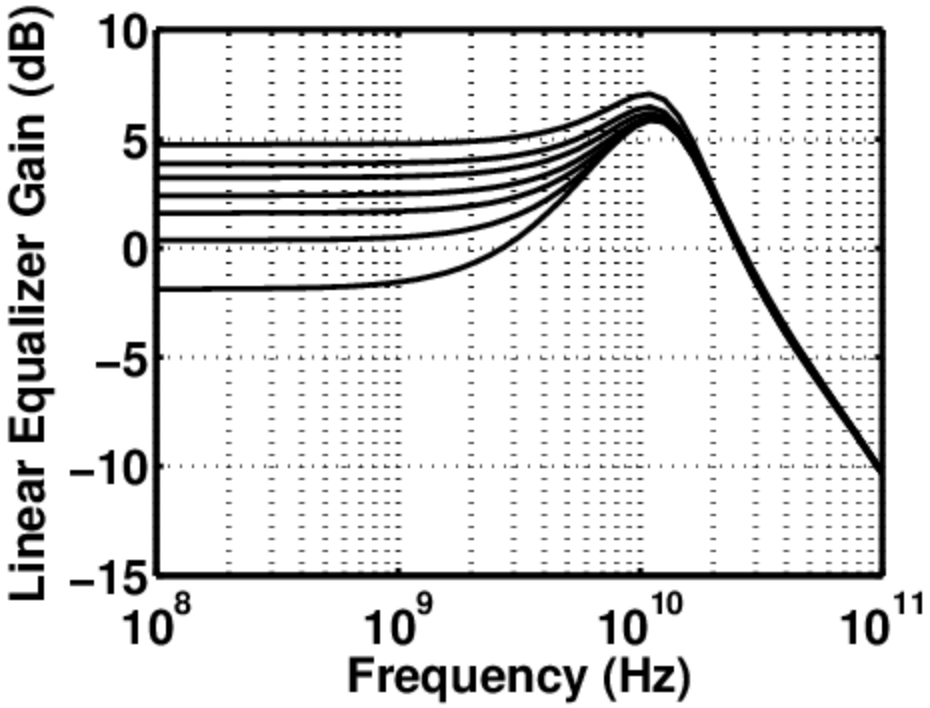
Complete Equalizer



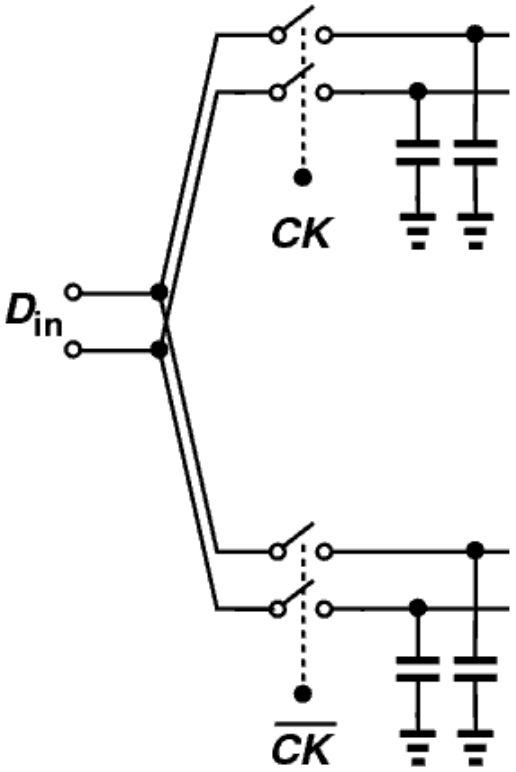
- Power Breakdown :
  - CTLE : 2.44 mW
  - DFE+RZ/NRZ Conv : 2.11 mW
  - Divider : 1.25 mW

CTLE Design

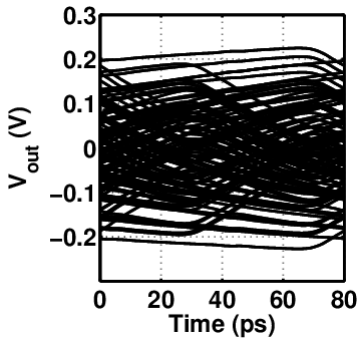


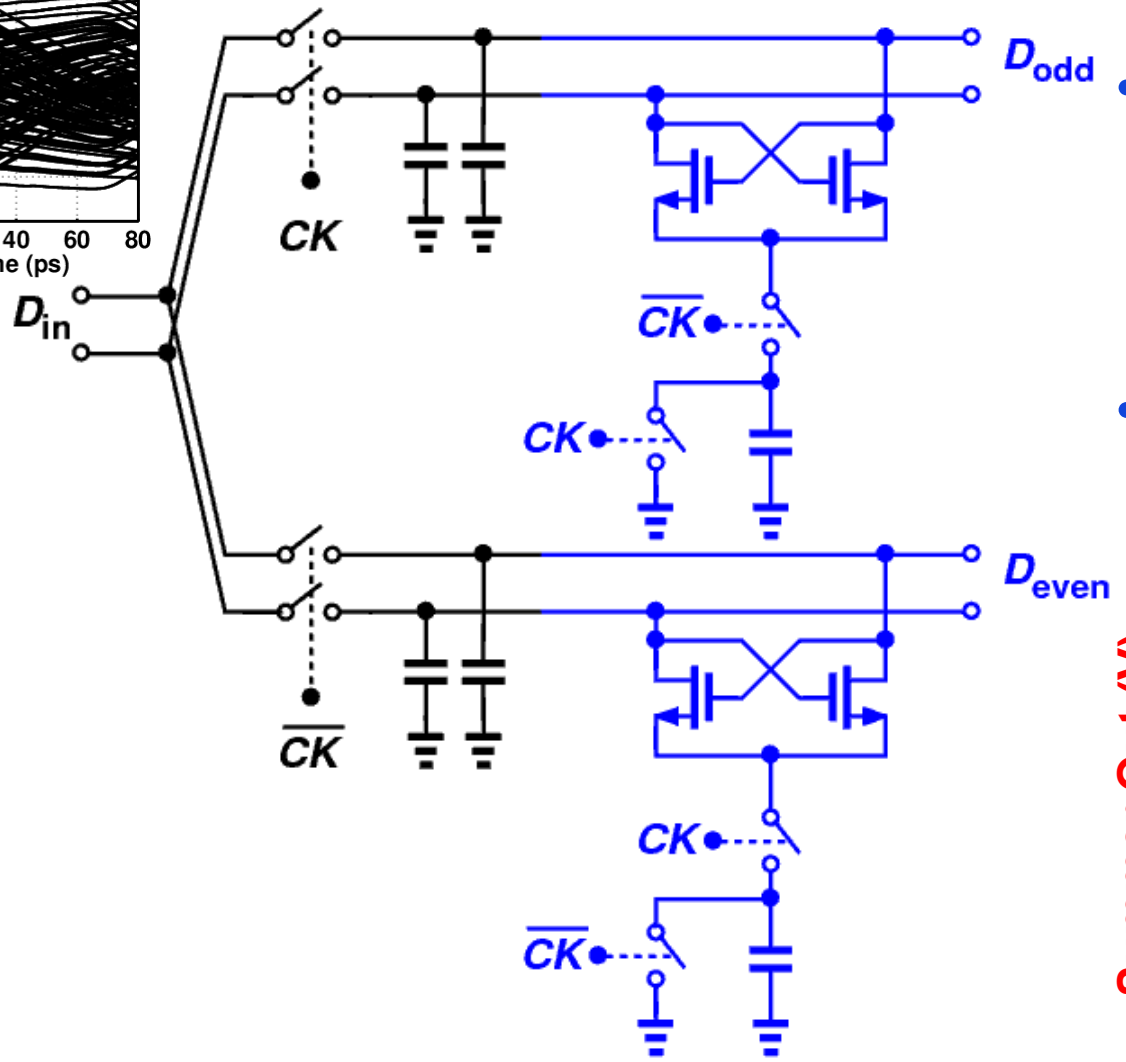


$DMUX_1$

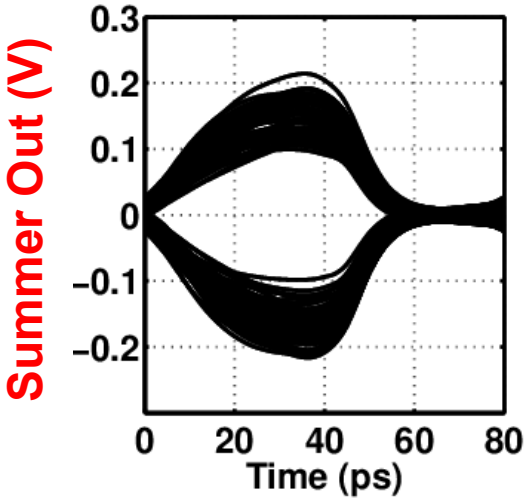


$DMUX_1$

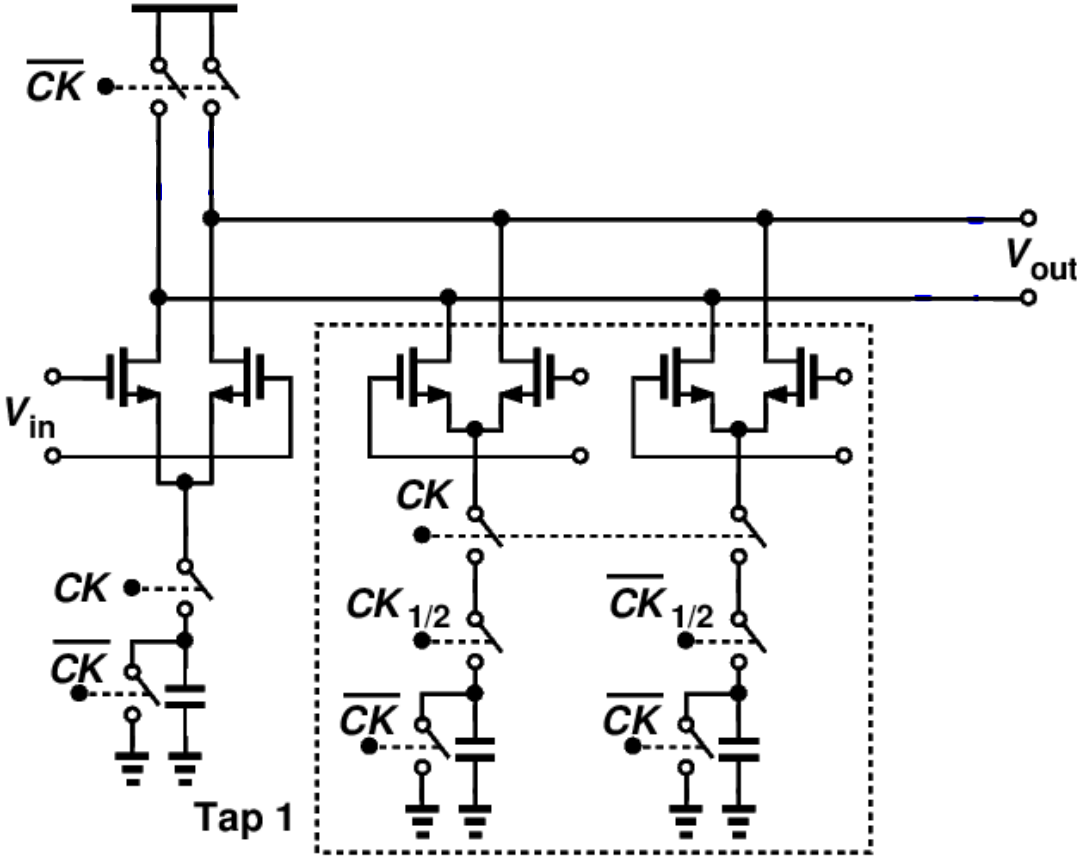




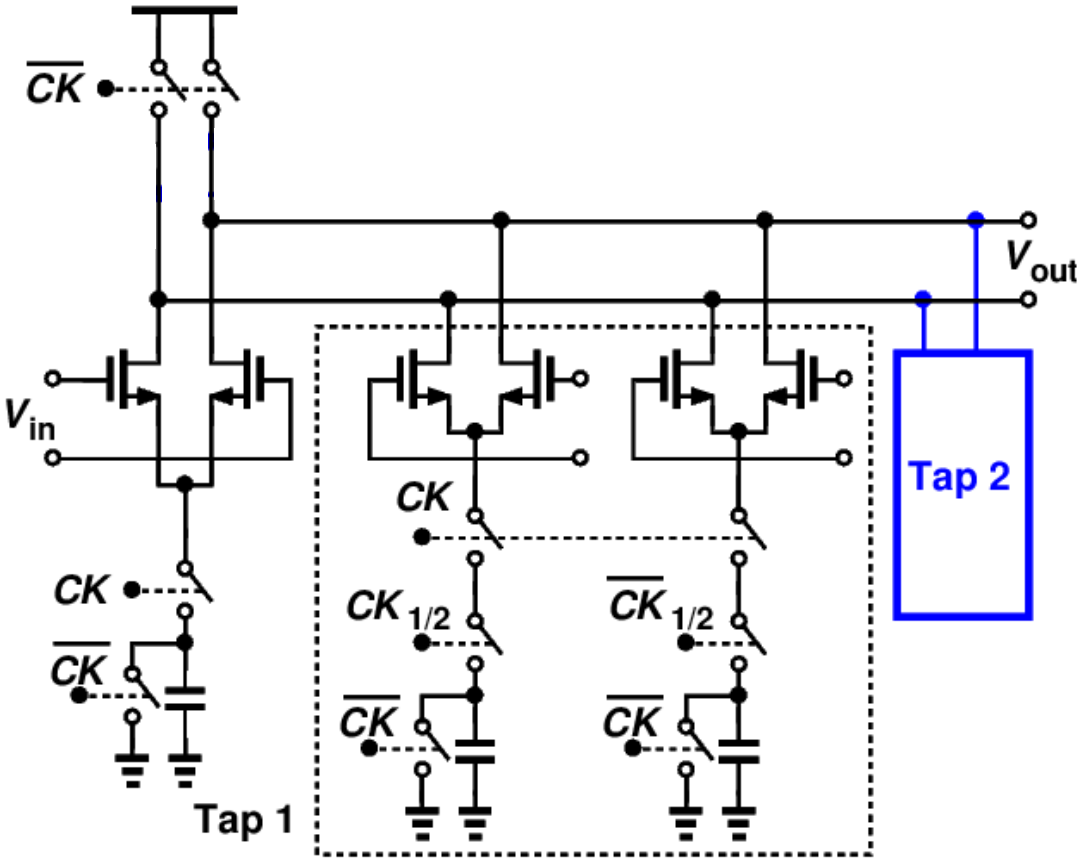
- Gain = 6 dB → Improves summer eye opening
- Linear enough : P_{1dB} = 180 mV_{pp}

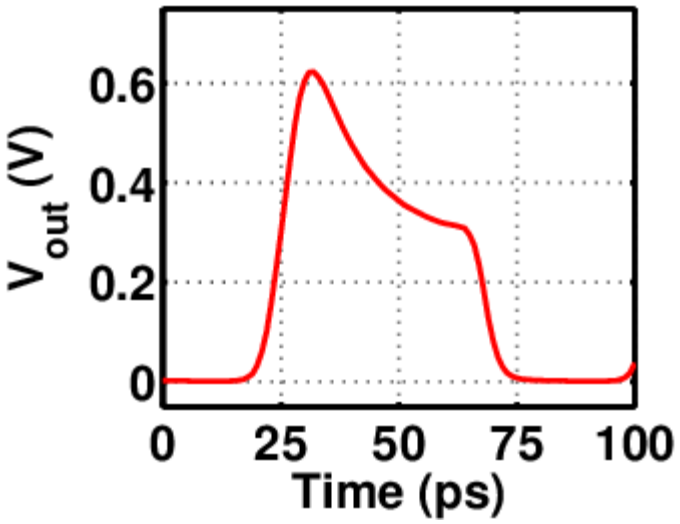


Charge-Steering Summer

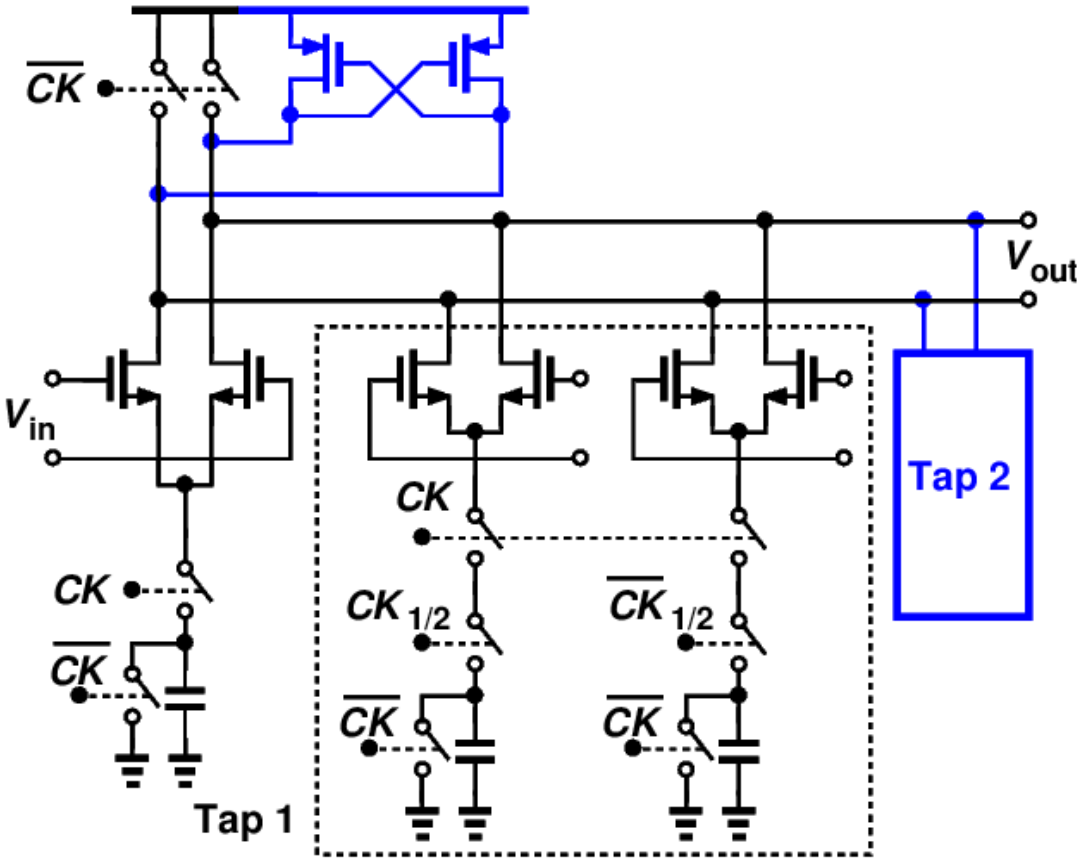


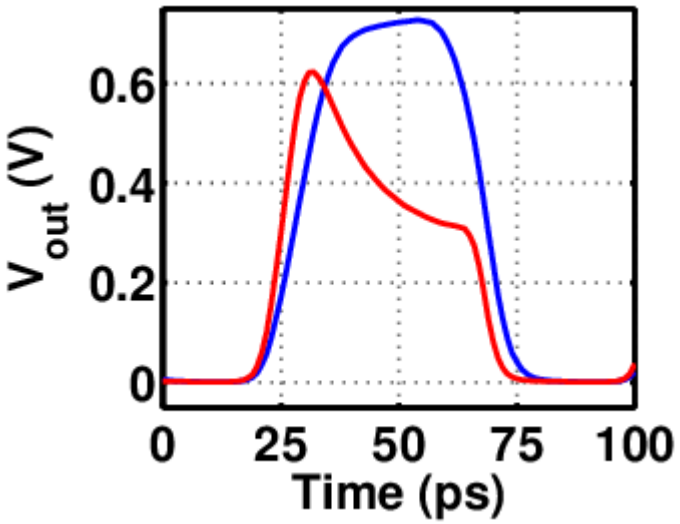
Charge-Steering Summer



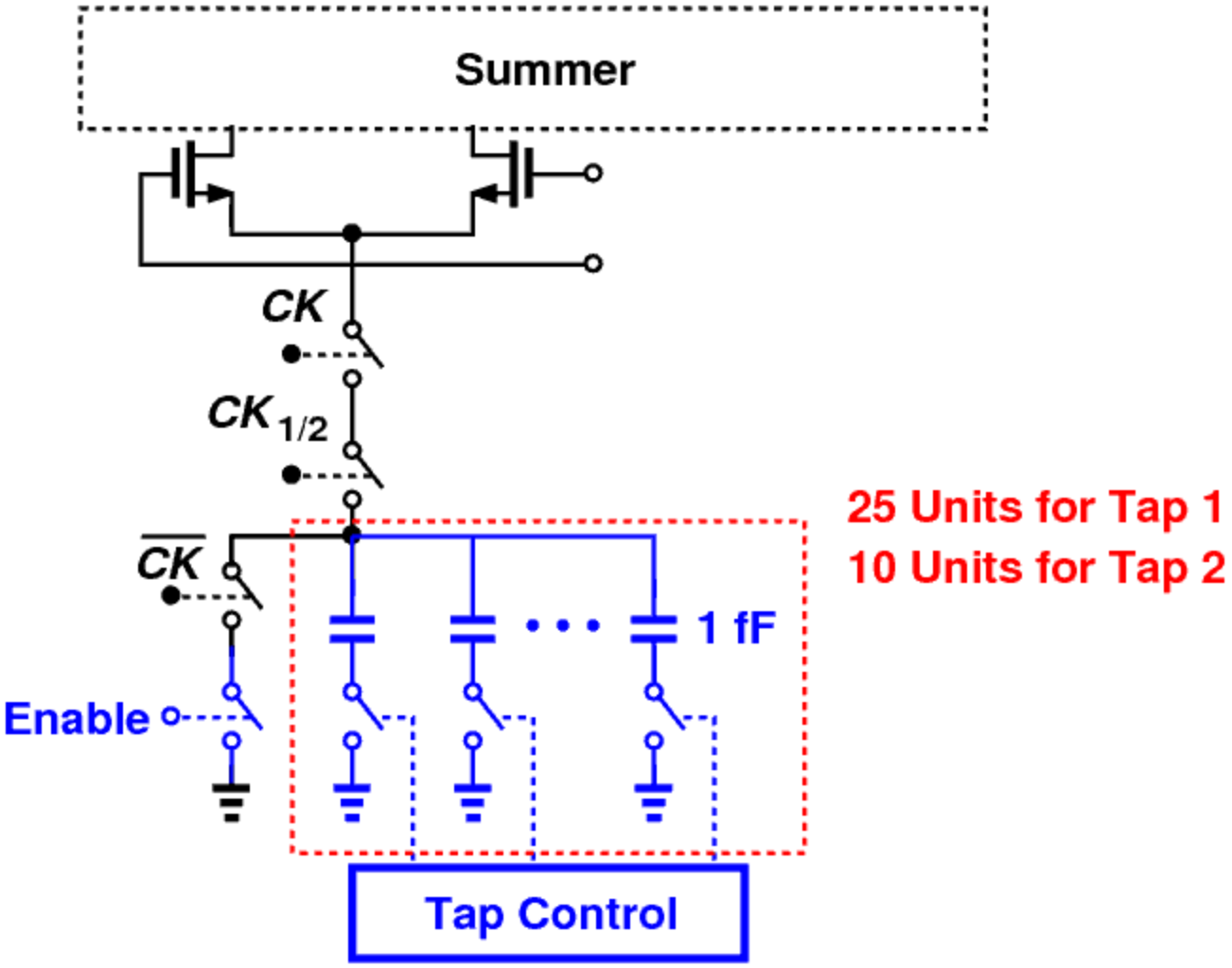


Charge-Steering Summer

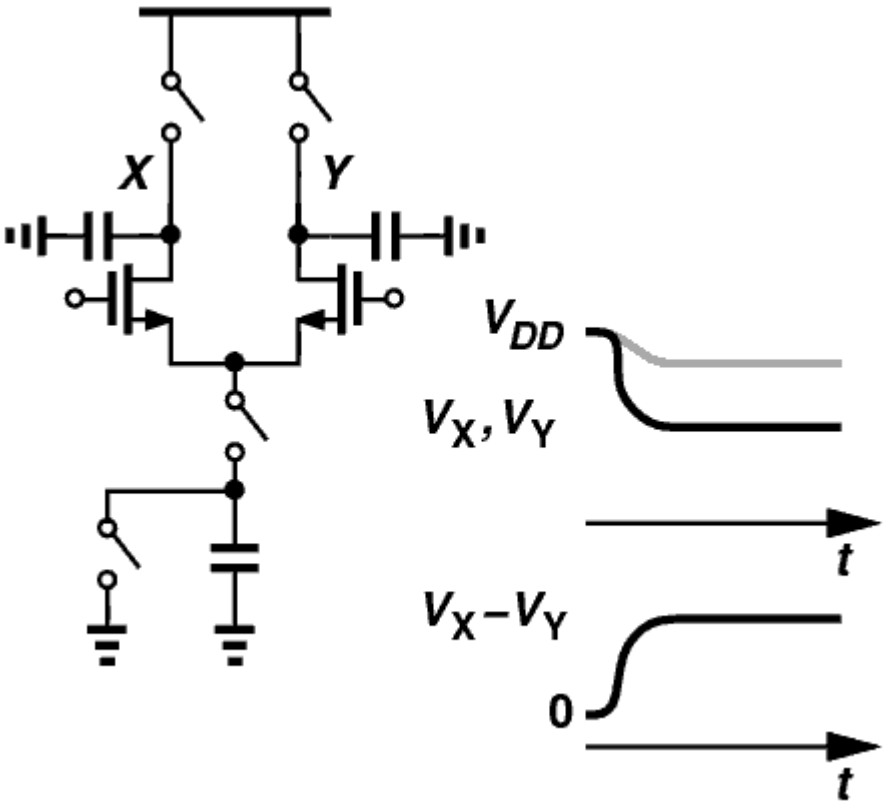




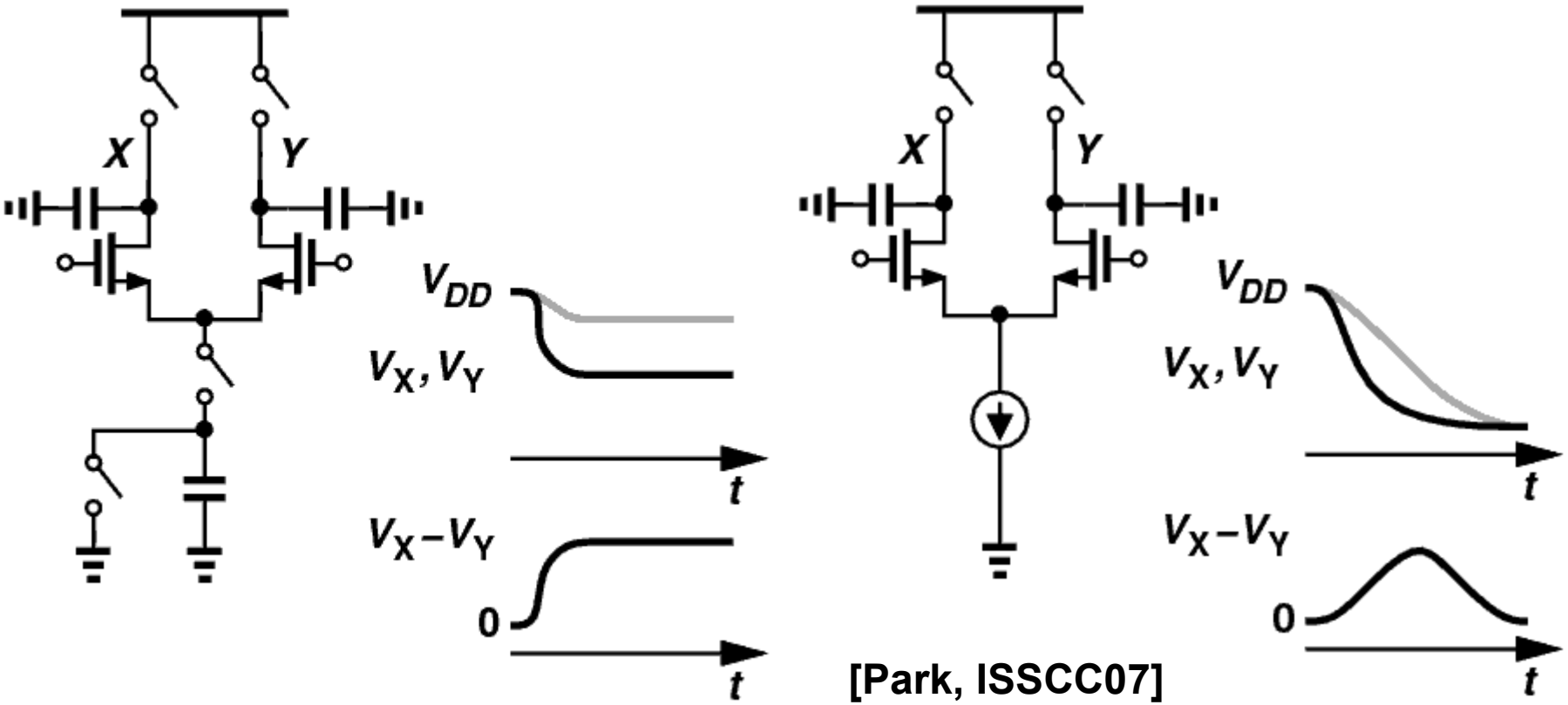
Feedback Tap Control



“Charge Steering” vs. “Current Integrating”

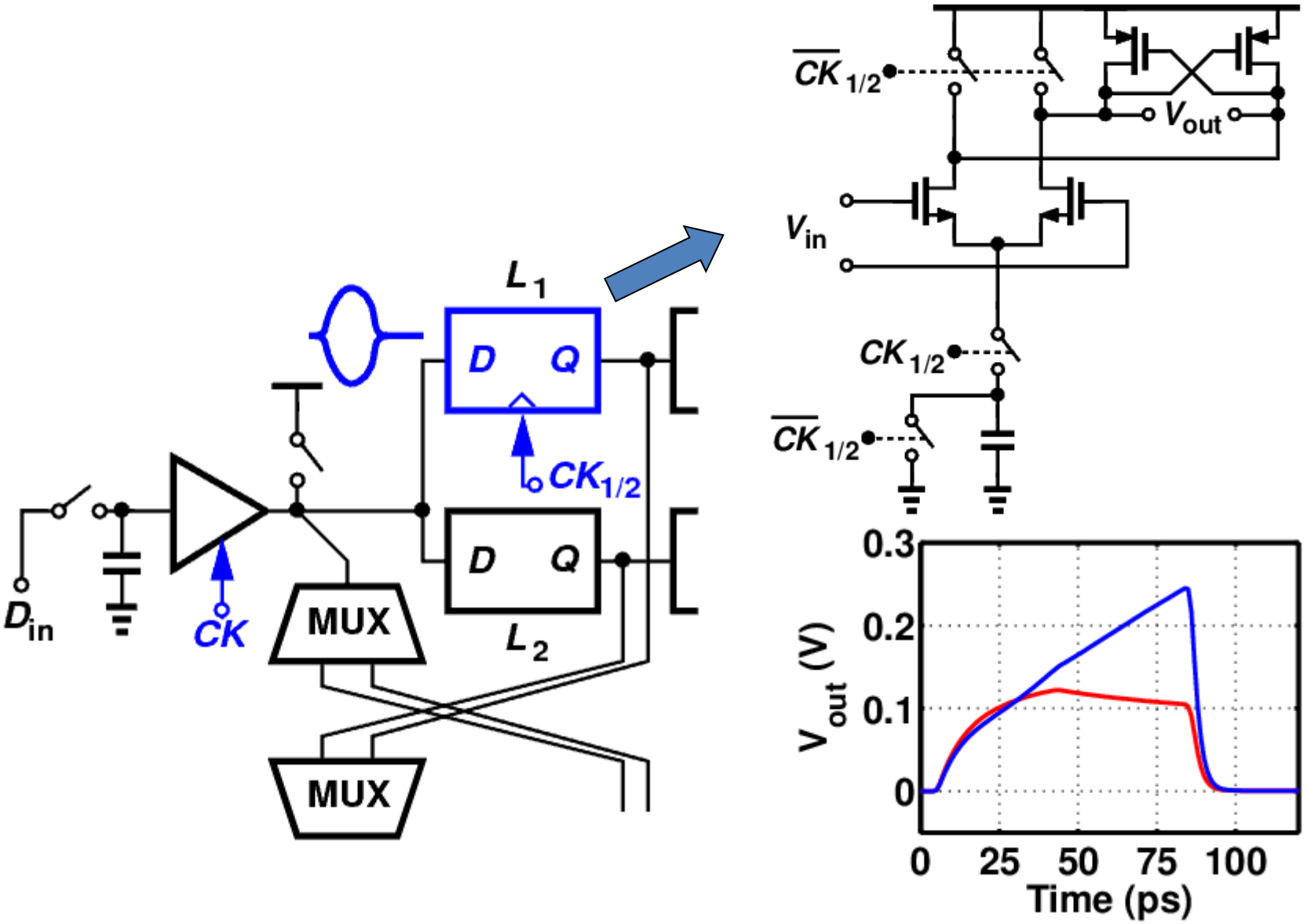


“Charge Steering” vs. “Current Integrating”

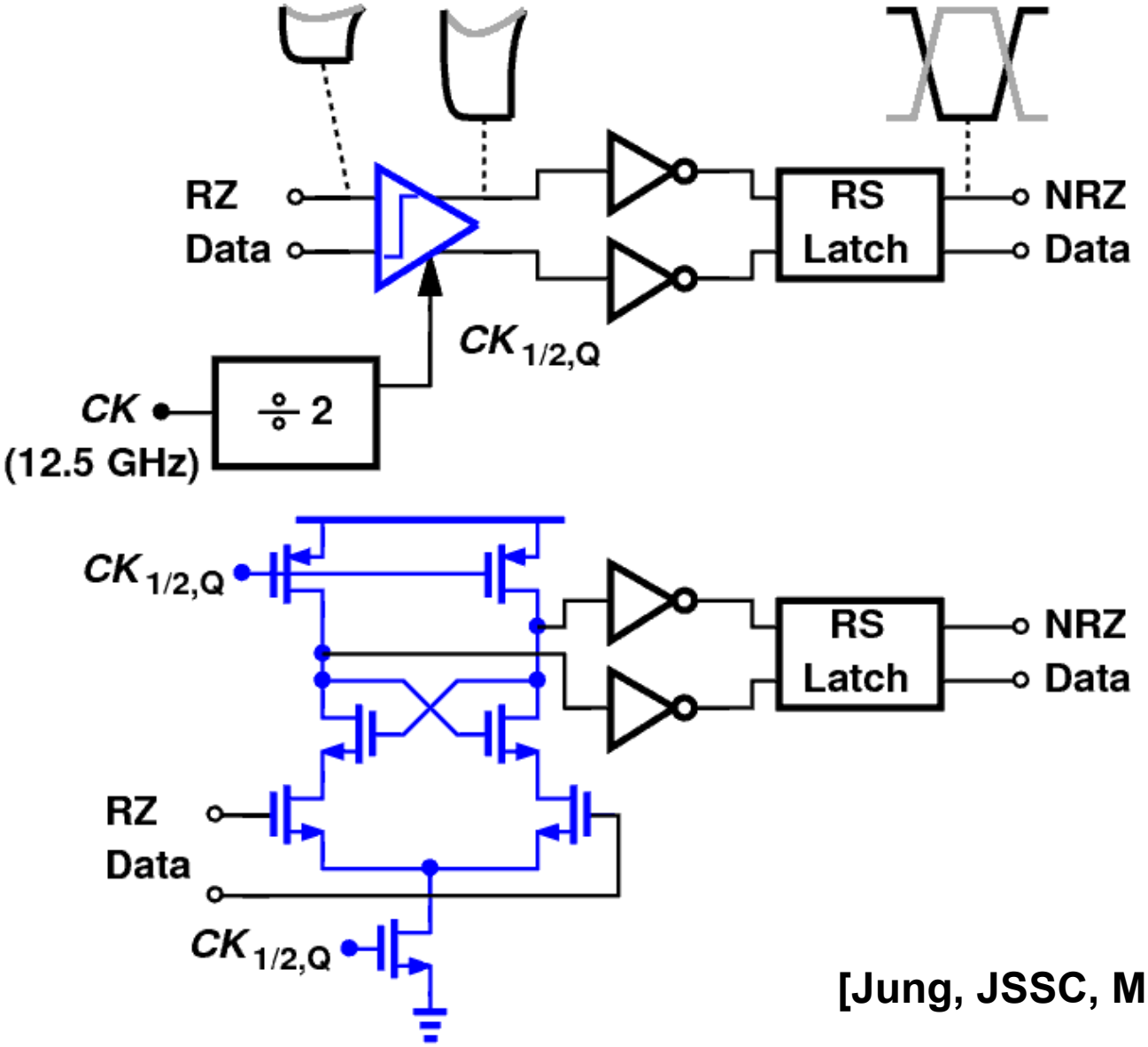


[Park, ISSCC07]

Latch with Improved Sensitivity

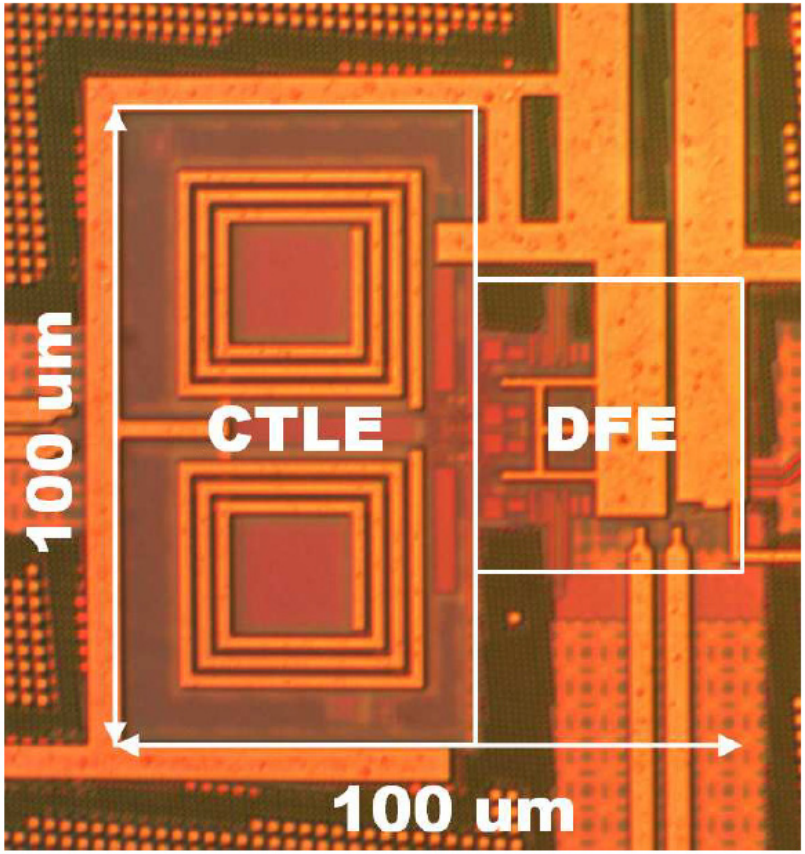


RZ/NRZ Conversion



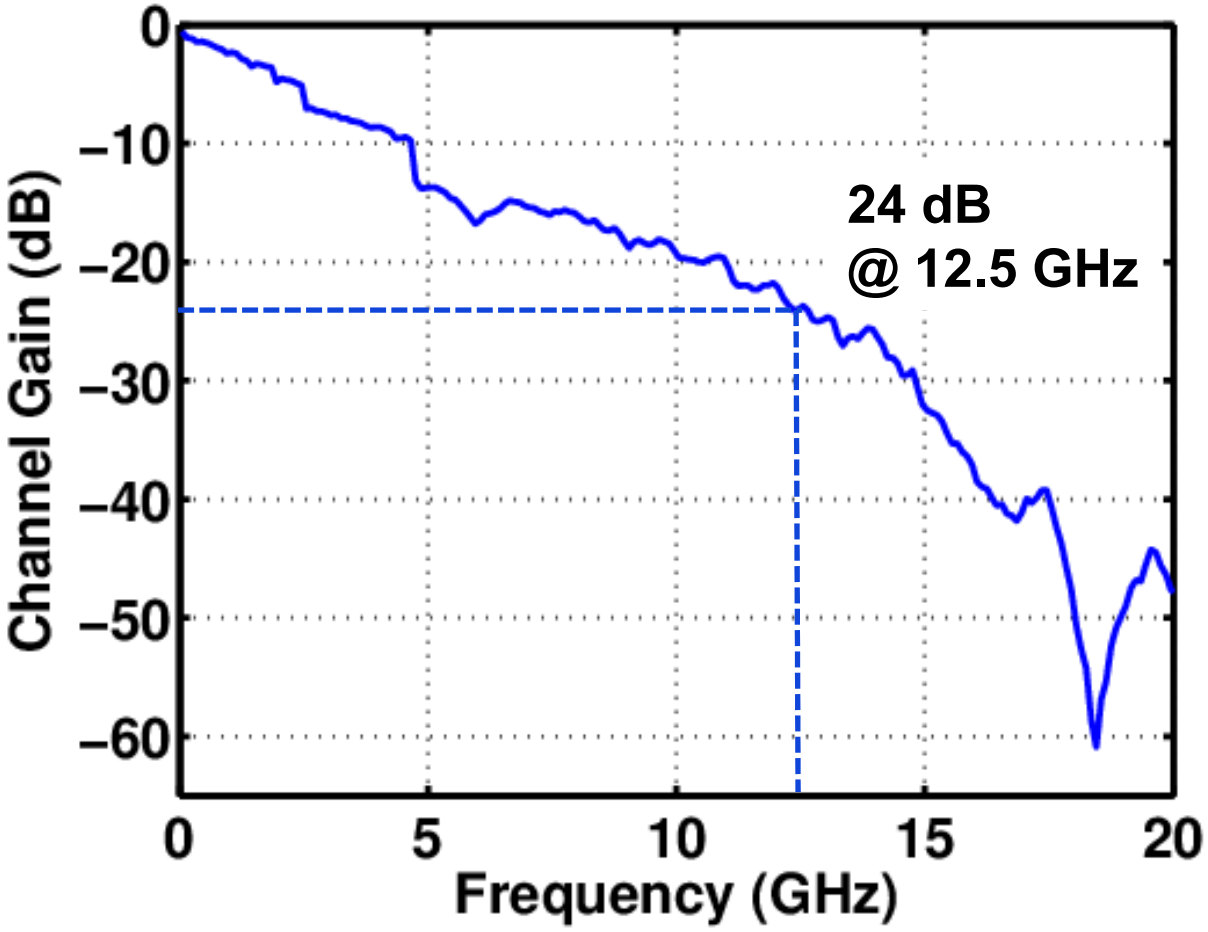
[Jung, JSSC, Mar. 13]

Equalizer Die Photograph



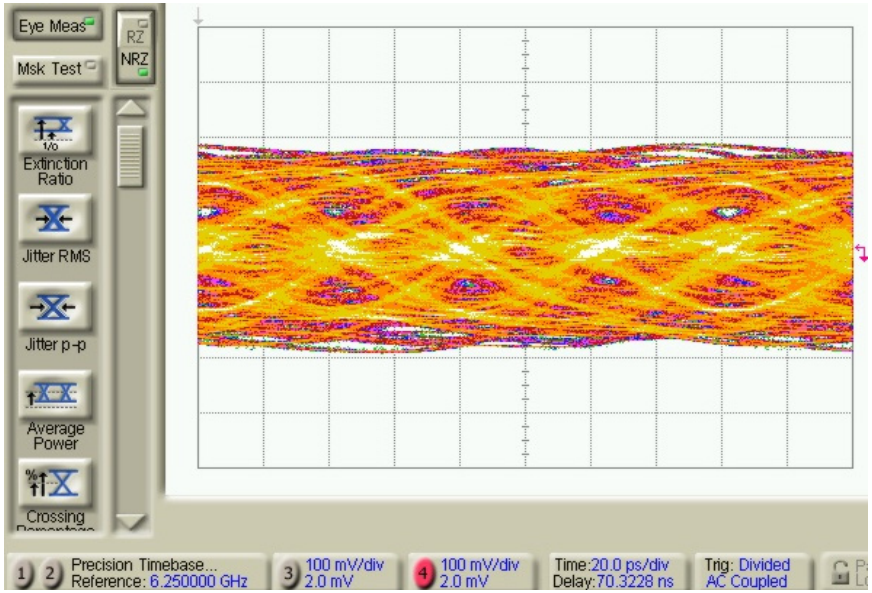
- Fabricated in TSMC's 45-nm digital CMOS process
- V_{DD} = 1V

Measured Channel Frequency Response

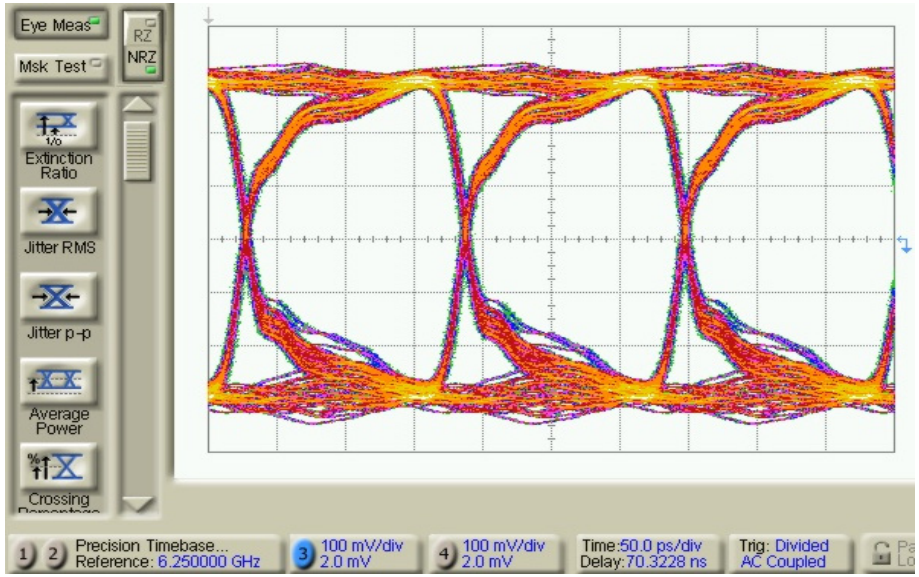


Measured Eye Diagrams

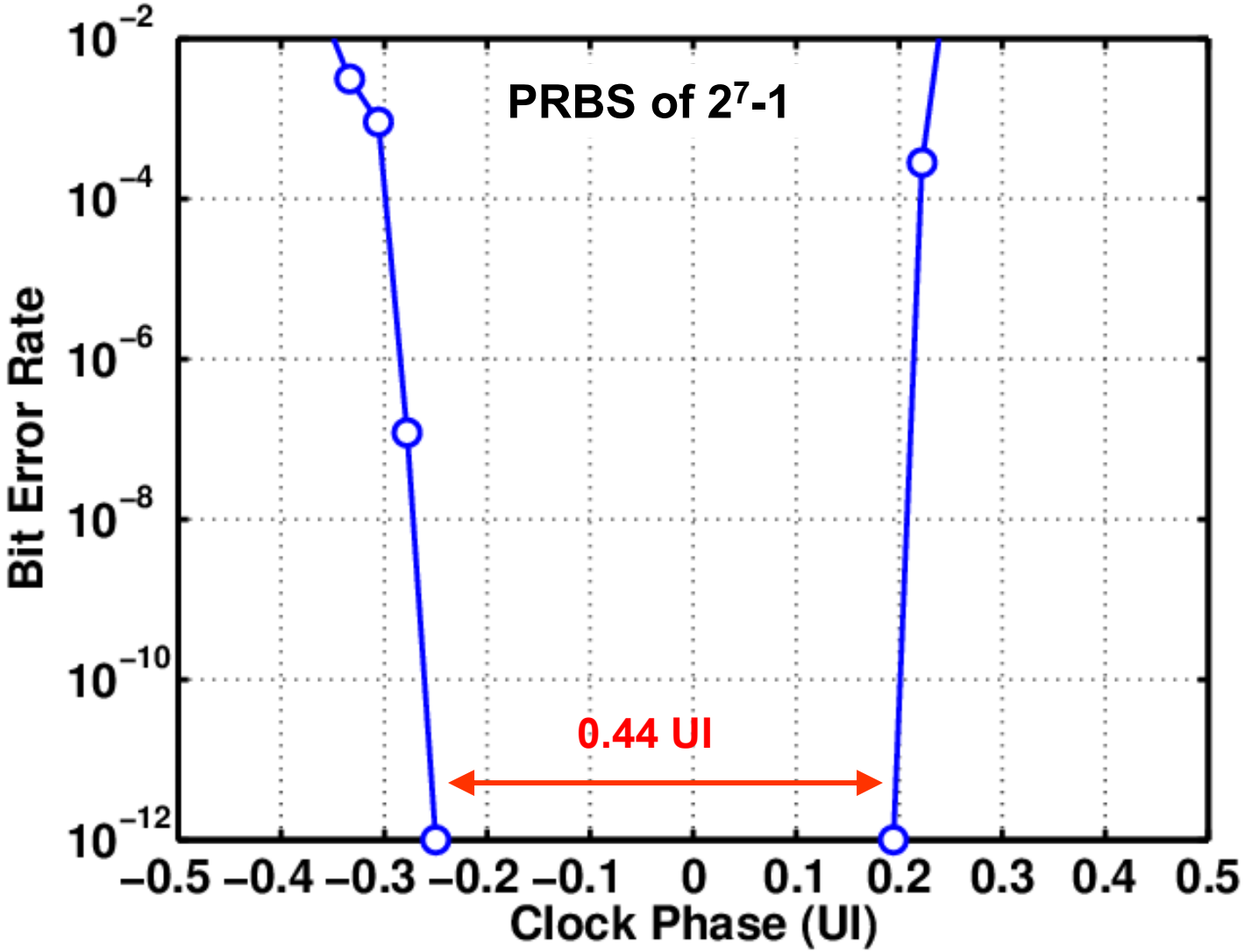
Channel Output



DMUXed Output (6.25 Gb/s)



Measured Bathtub Curve



Performance Summary

Reference	A. Agrawal ISSCC 2012	J. Bulzacchelli ISSCC 2012	K. Jung ISSCC 2013	K. Kaviani CICC 2012	J. E. Proesel VLSI 2011	This Work
Data Rate	19 Gb/s	28 Gb/s	22 Gb/s	27 Gb/s	20 Gb/s	25 Gb/s
Architecture	4–tap FFE + 5–tap DFE	CTLE + 15–tap DFE	CTLE + 2–tap DFE	1–tap DFE	CTLE + 1–tap DFE	CTLE + 2–tap DFE
DFE Clocking	Quarter Rate	Half Rate	Quarter Rate	Quarter Rate	Half Rate	Half Rate
Channel Loss @ Nyquist	25 dB	35 dB	16 dB	>10 dB	26.3 dB	24 dB
BER / Horizontal Eye Opening	$< 10^{-9}$ / 36 % UI	$< 10^{-9}$ / 35.6 % UI	$< 10^{-12}$ / 26 % UI	$< 10^{-9}$ / 26 % UI	$< 10^{-8}$ / 26 % UI	$< 10^{-12}$ / 44 % UI
Supply (V)	1.1	1.05	1.15	1.1	1.2	1
Power (mW)	118	80 *	20.6	11.1	13.2	5.8
Area (mm^2)	0.07	0.81**	0.016	0.015	0.012	0.01
Technology	45–nm SOI CMOS	32–nm SOI CMOS	45–nm CMOS	40–nm CMOS	45–nm SOI CMOS	45–nm CMOS

*Only for odd and even DFEs. Excludes CTLE, etc.

**Includes TX+RX+PLL/4

Performance Summary

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Technology	45–nm SOI CMOS	32–nm SOI CMOS	45–nm CMOS	40–nm CMOS	45–nm SOI CMOS	45–nm CMOS

*Only for odd and even DFEs. Excludes CTLE, etc.

**Includes TX+RX+PLL/4

Conclusion

- Charge steering affords low power consumption at high speeds.
- Half-rate/quarter-rate DFE with front-end DMUX lends itself to charge-steering implementations.
- Merged MUX and feedback Gm avoids reset phase and allows t_{cq} < 1 UI.
- An equalizer has been realized with 4X improvement in energy efficiency.

Acknowledgment

- Research supported by Texas Instruments and Realtek Semiconductor.
- We gratefully acknowledge the TSMC University Shuttle Program for chip fabrication.

A 0.25pJ/b 0.7V 16Gb/s 3-Tap Decision-Feedback Equalizer in 65nm CMOS

Rui Bai[1], Samuel Palermo[2], Patrick Chiang[1,3]

[1] Oregon State University, Corvallis, OR

[2] Texas A&M University, College Station, TX

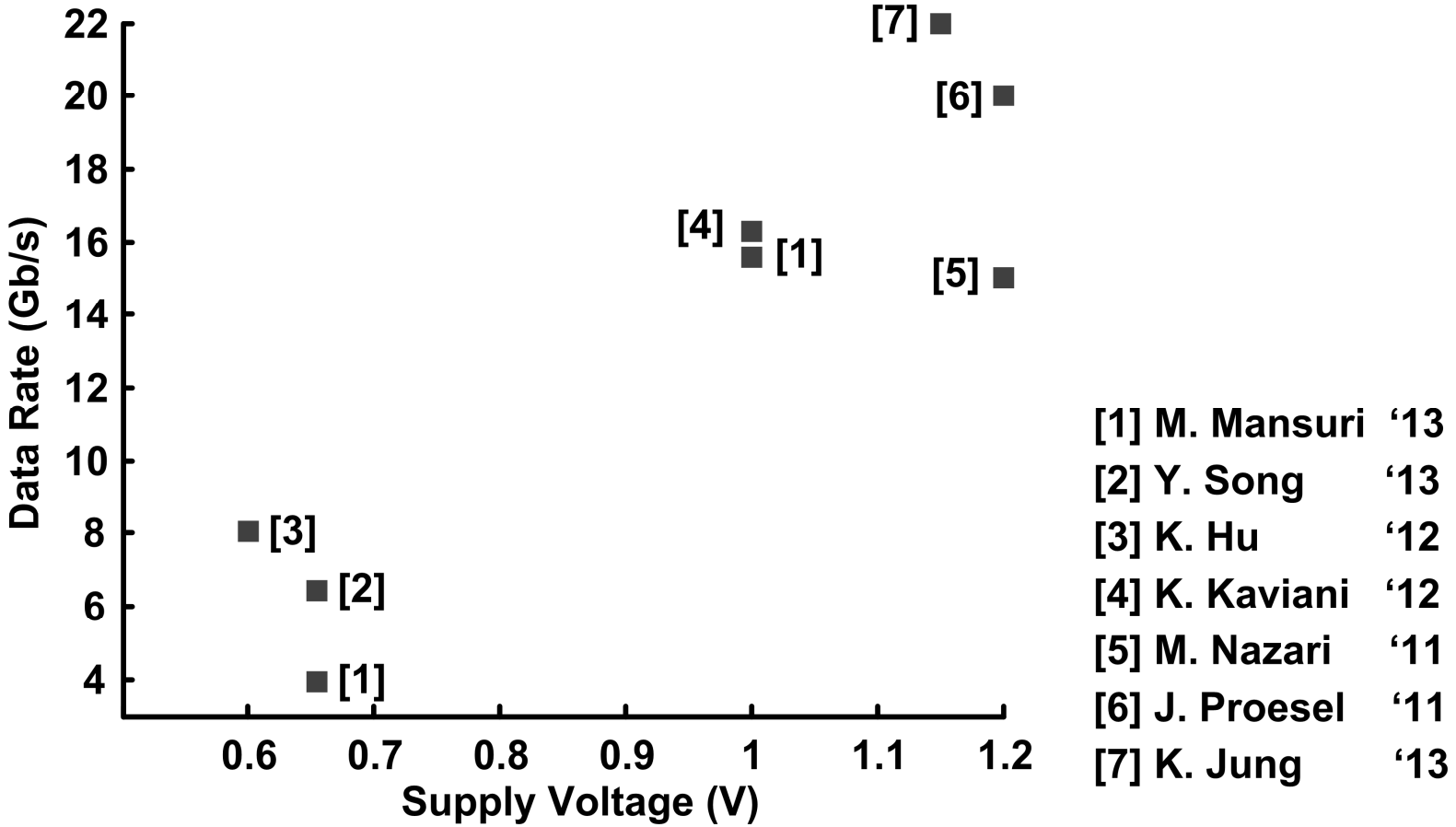
[3] Fudan University, Shanghai, China

Outline

- **Motivation for low-V_{DD} DFE**
- **Architecture of proposed DFE**
- **Low-V_{DD} DFE design challenges**
- **Measurement results**
- **Conclusions**

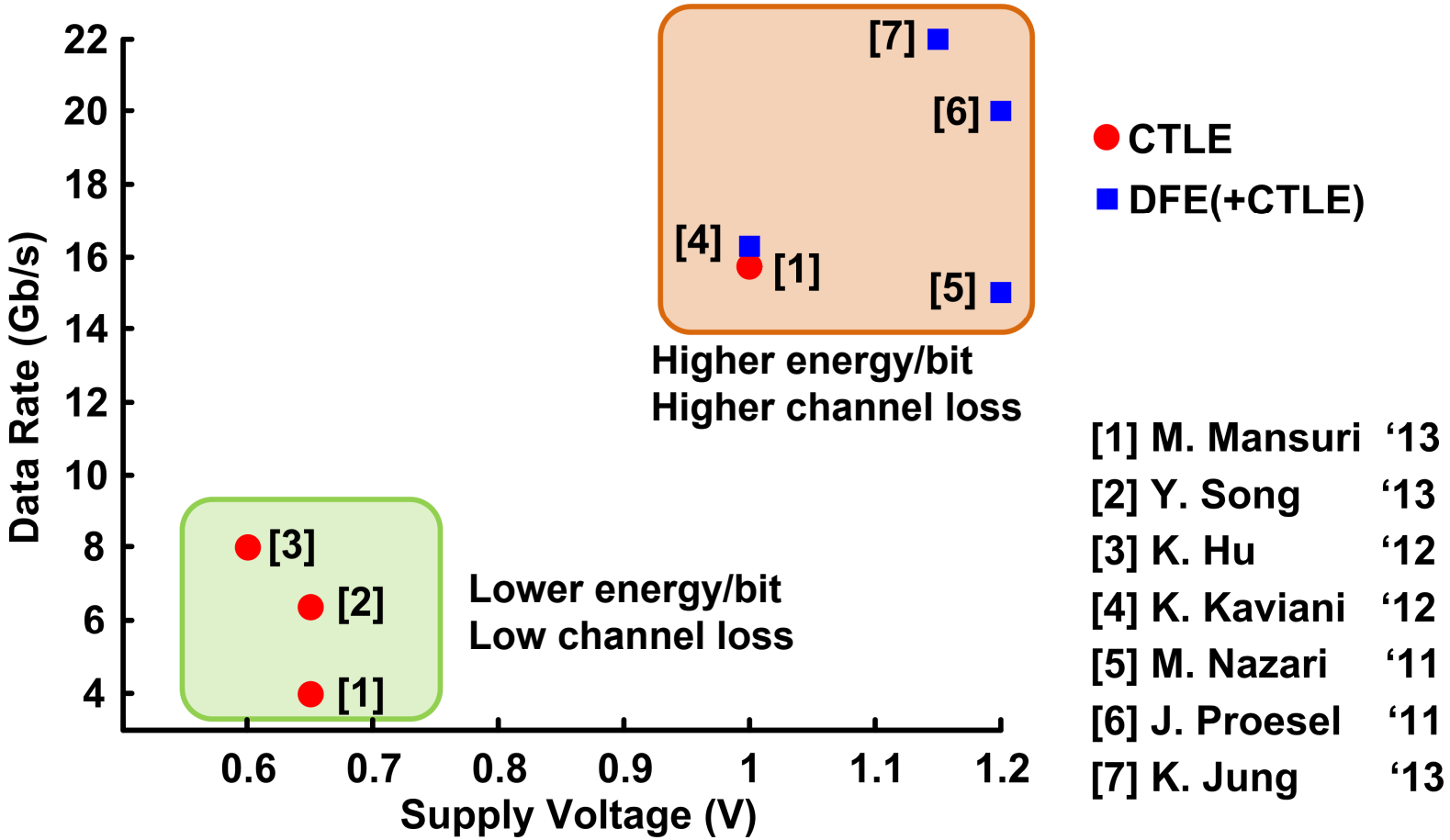
Motivation

Recently Published Receivers with Energy-Efficiency < 1pJ/bit



Motivation

Recently Published Receivers with Energy-Efficiency < 1pJ/bit



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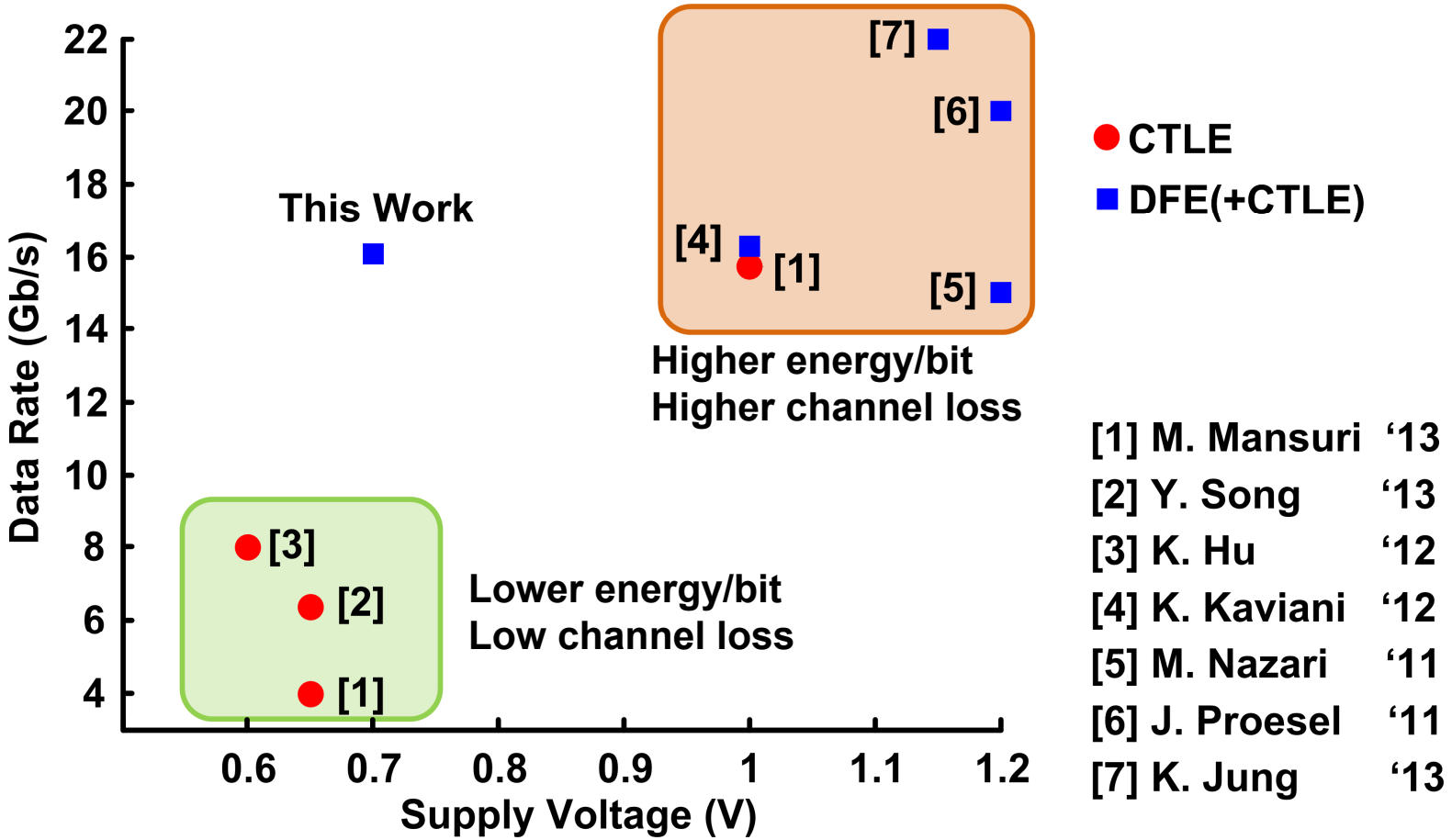


Our Goal: Low-V_{DD}, 15Gbps+ Decision-Feedback Equalizer

Outline

- Motivation for low-V_{DD} DFE
- Architecture of proposed DFE
- Low-V_{DD} DFE design challenges
- Measurement results
- Conclusions

DFE Architecture

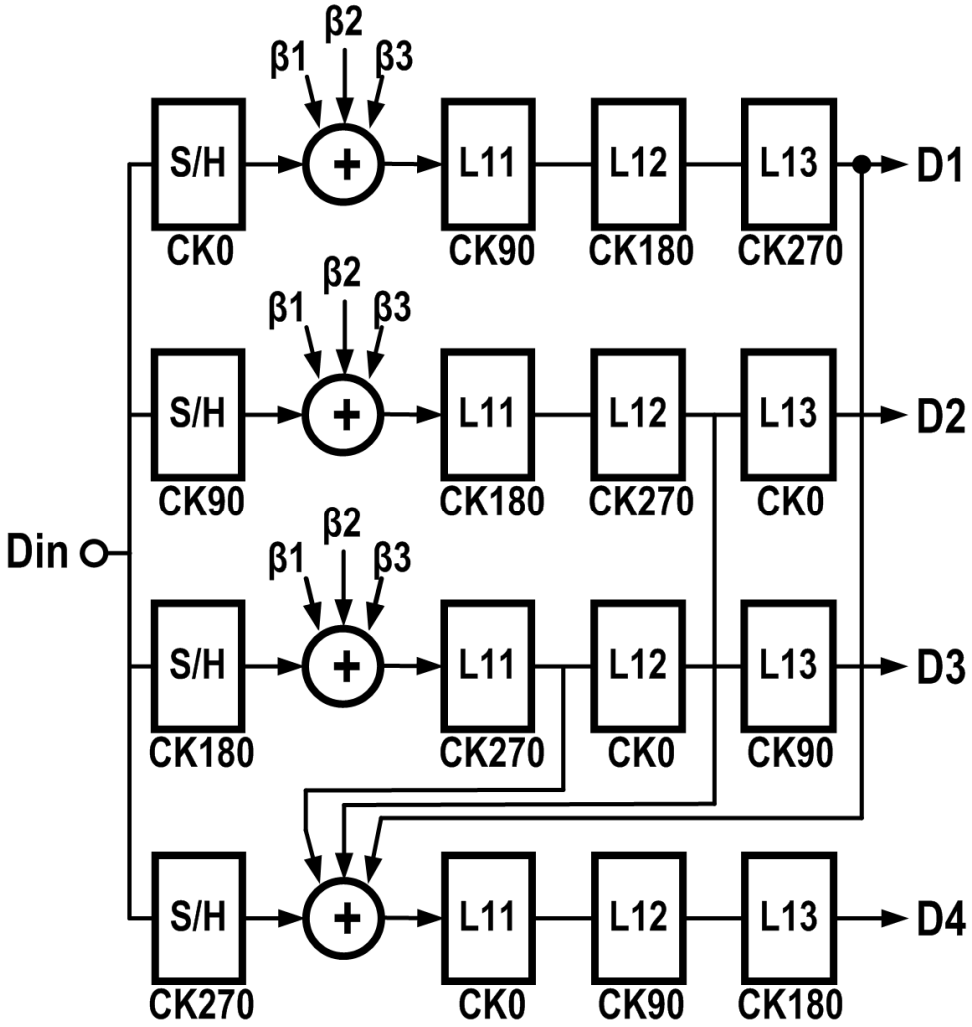
- 1:4 DEMUX

* Overcome speed limit at low-V_{DD}

* Quarter-rate CMOS clocking

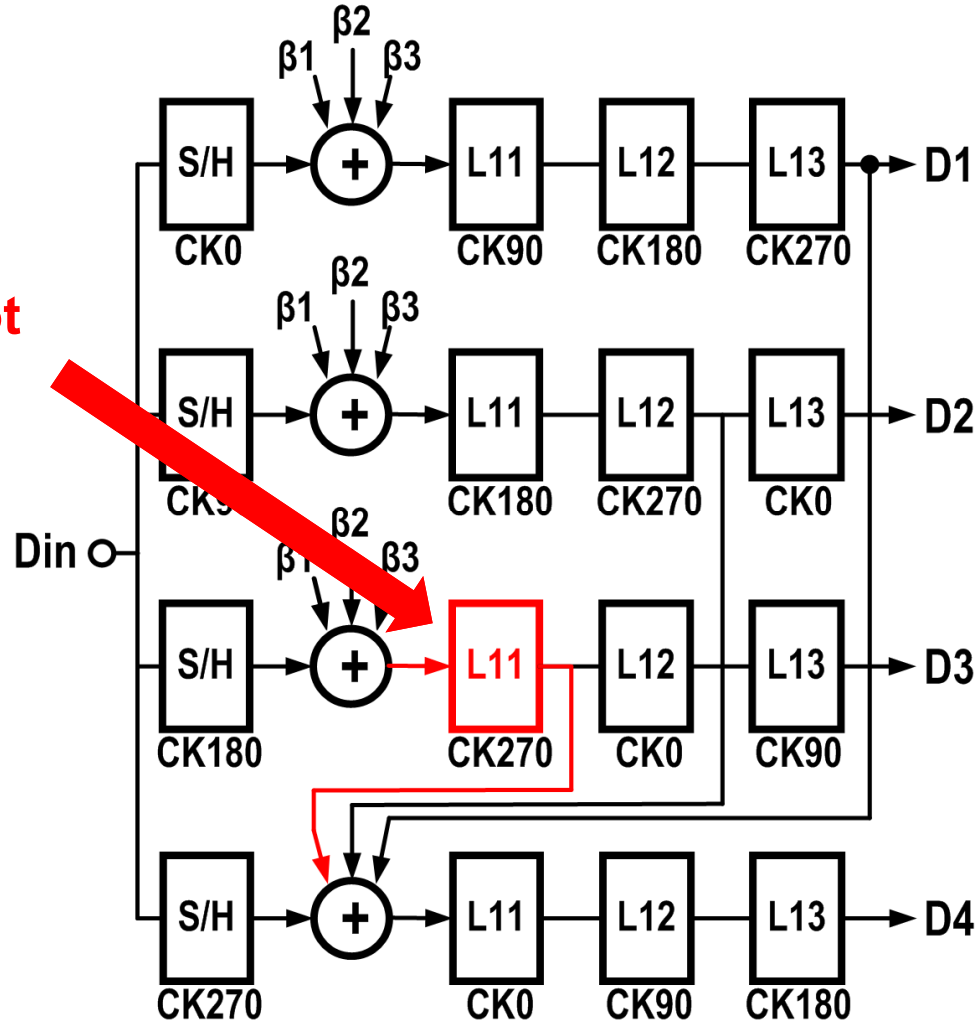
- 3-tap direct feedback

* Loop unrolling needs 32 slicers

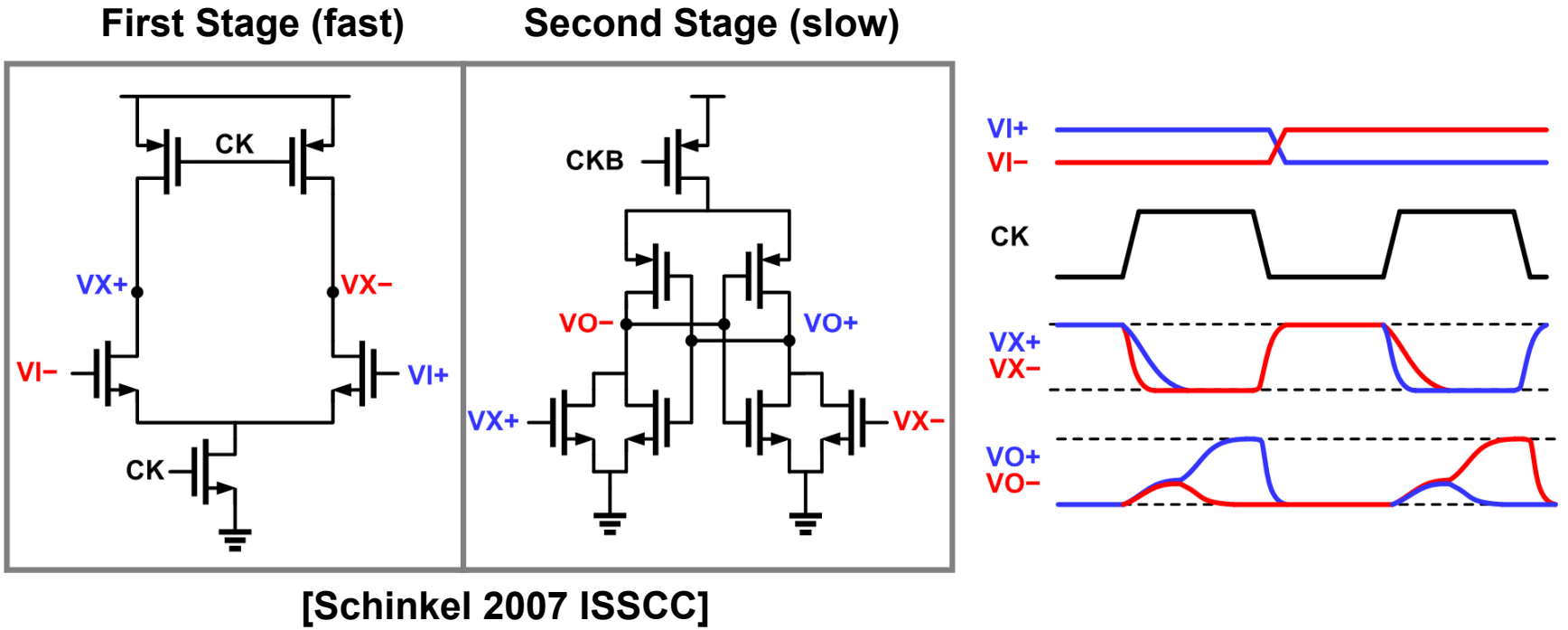


Low-V_{DD} DFE Design Challenges

- Latch
  - 1-UI critical path delay is not relaxed by 1:4 DEMUX
- S/H
- Summer



Conventional Regenerative Latch



[Schinkel 2007 ISSCC]

☺ Fast first stage → small aperture time

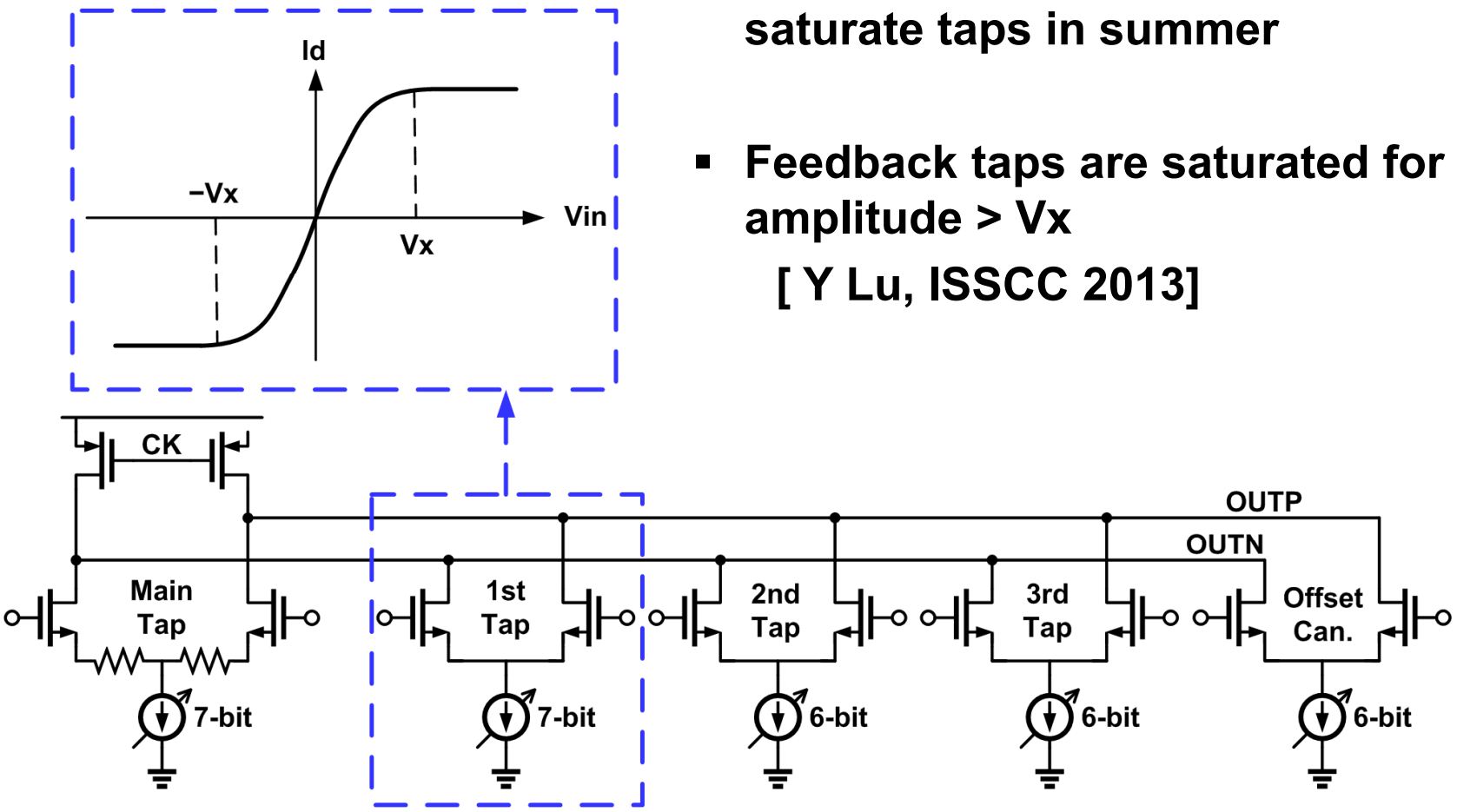
☹ Slow second stage regeneration → large delay

☺ Full-swing output

Reducing the Latch Output Swing

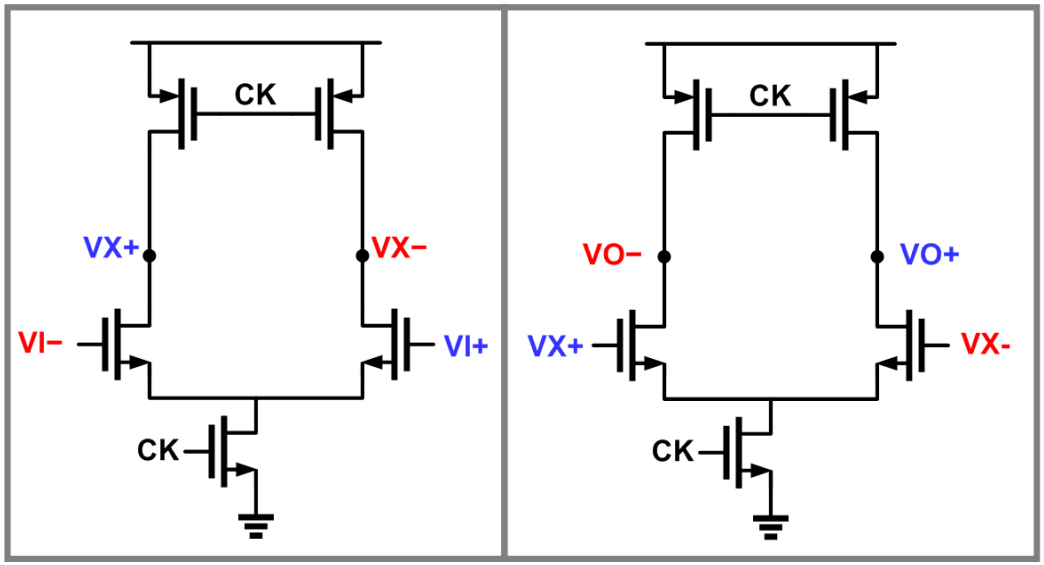
- Latch output voltage only needs to saturate taps in summer
- Feedback taps are saturated for input amplitude > Vx

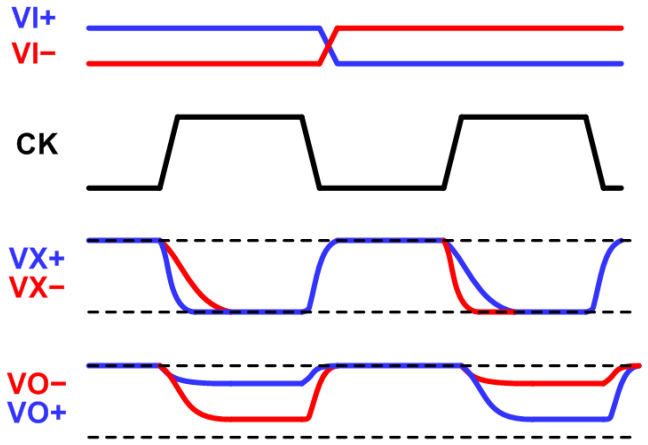
  [Y Lu, ISSCC 2013]



Faster Latch with Reduced Output Swing

First Stage (fast) Second Stage (fast)





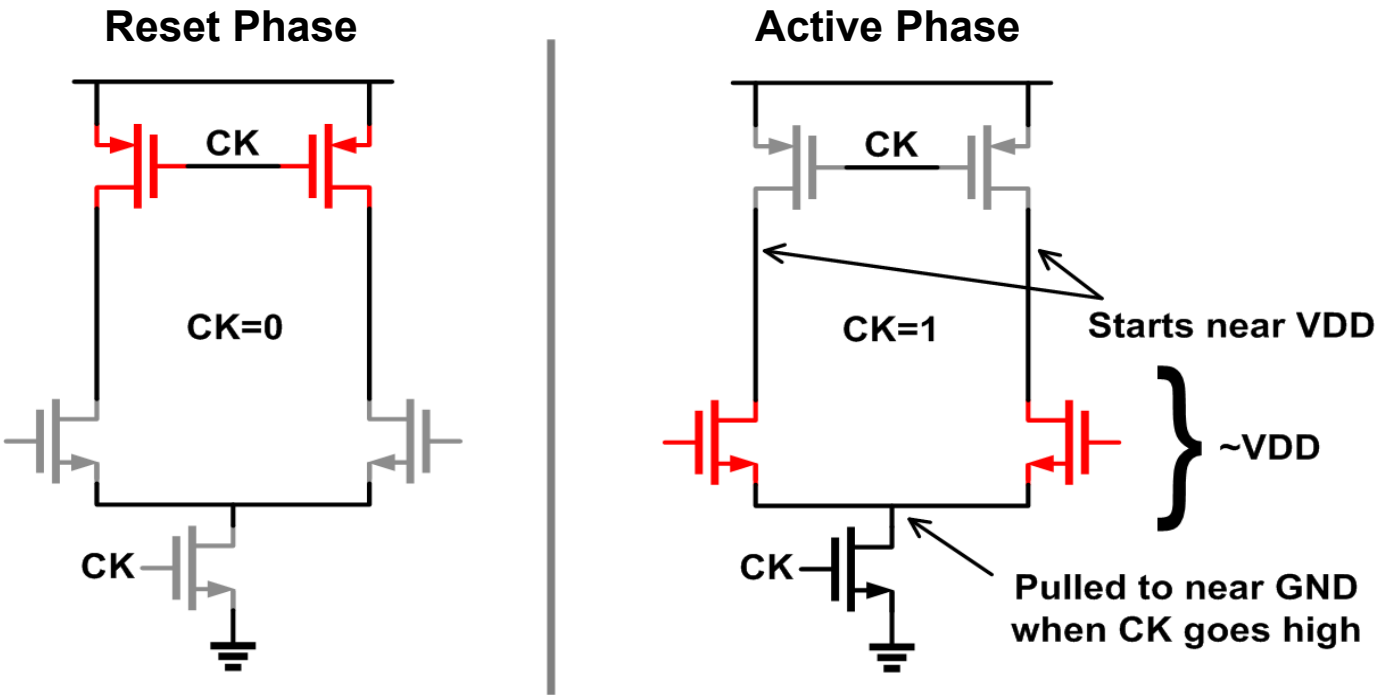
*Similar to [S. Chiang 2013 VLSI]

☺ Fast first stage → small aperture time

☺ Fast second stage→ small delay

☹ Output not full-swing

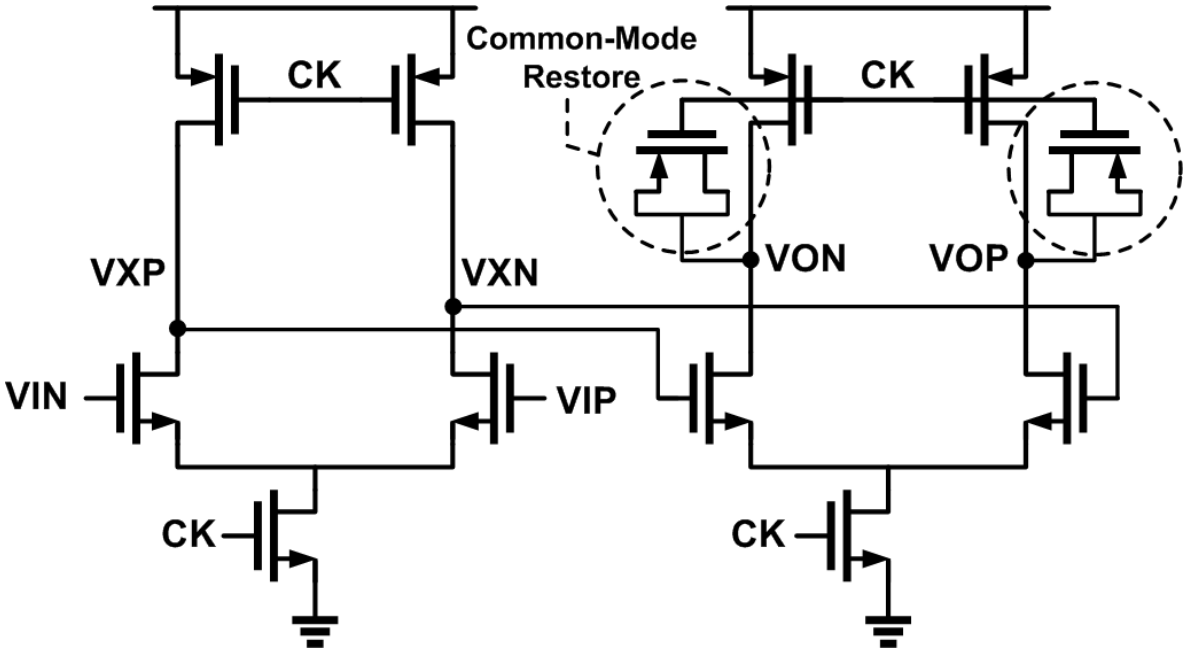
Latch Headroom at Low-V_{DD}



Only one stack of headroom needed

- **Maximize g_m for active transistors**
- **Enables further voltage scaling**

Charge-Based Low-Swing Latch

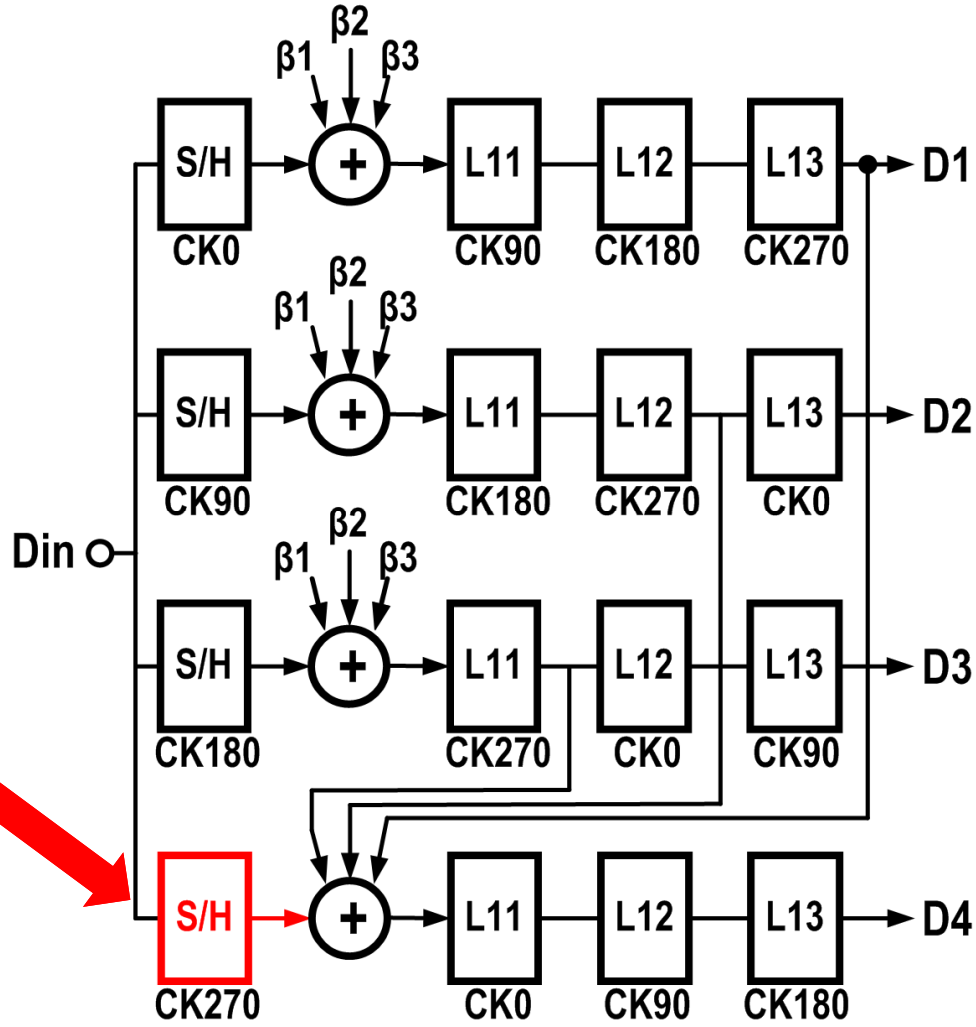


- Differential output swing is proportional to output voltage common-mode (V_{CM}) drop
- V_{CM} drop is limited by input level of following stage

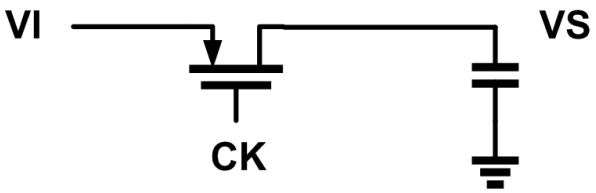
→ Boosting V_{CM} allows for larger gain

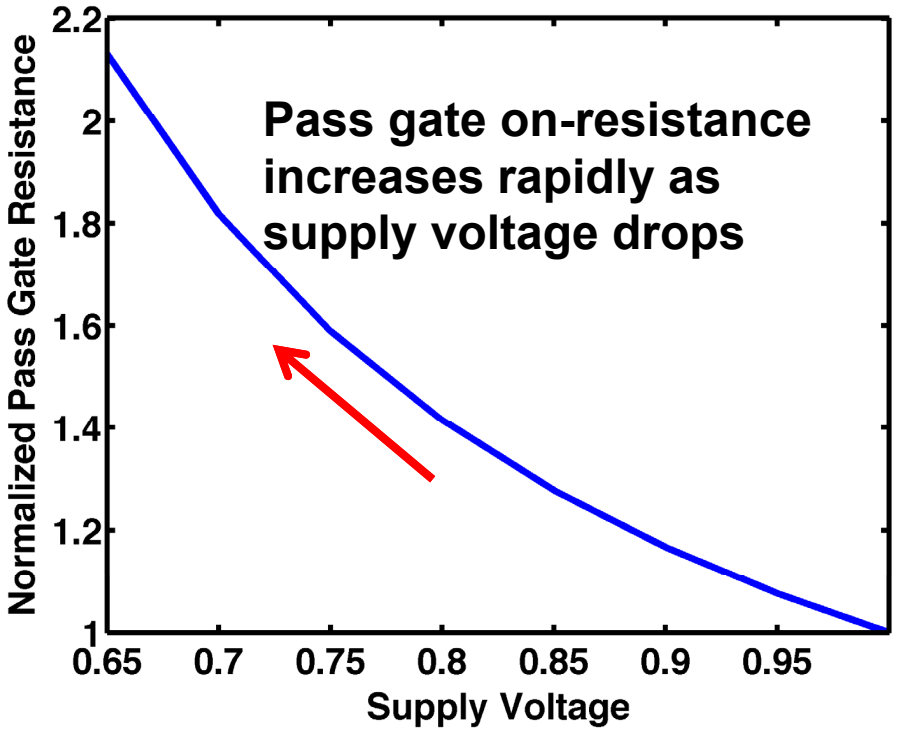
Low-V_{DD} DFE Design Challenges

- Latch
- S/H
  - BW and sampling aperture degradation
- Summer



S/H Performance Degradation at Low-V_{DD}

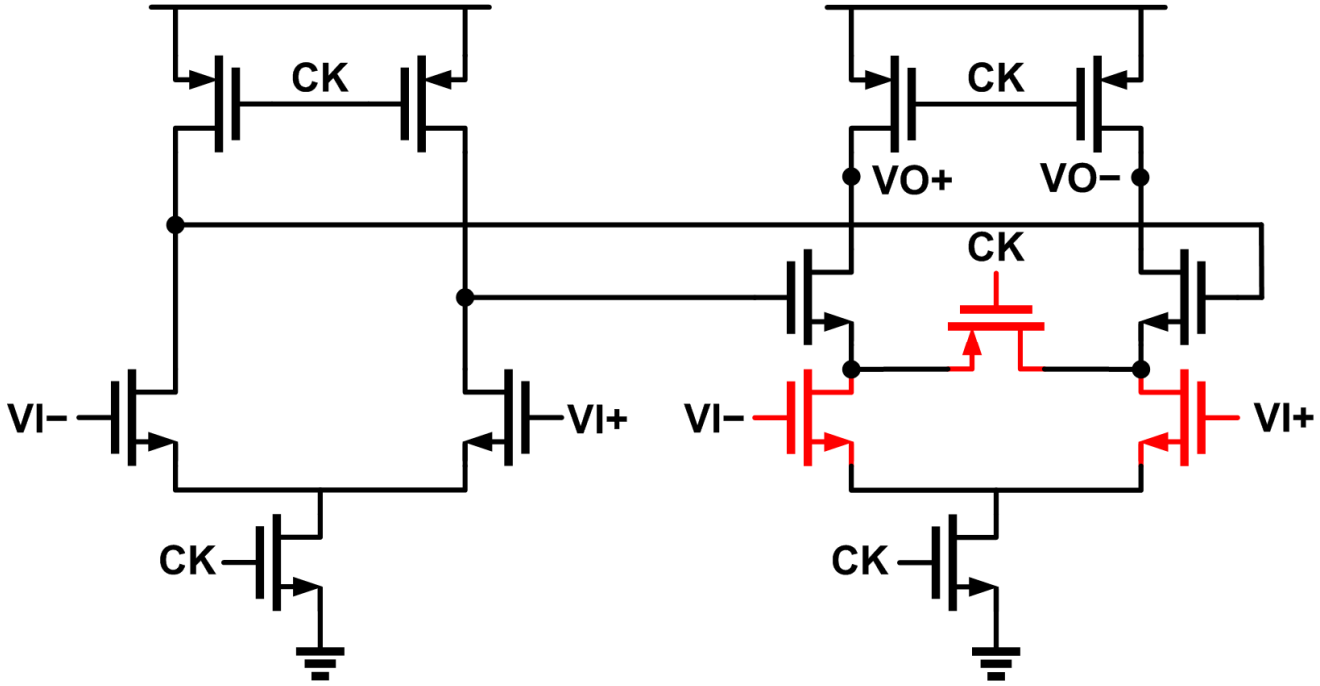




Pass-gate S/H:

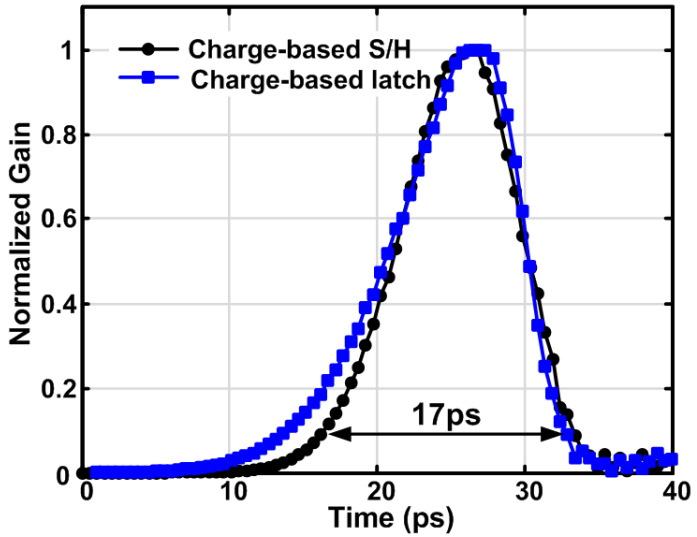
- **Bandwidth is severely degraded at low VDD**
- **Sampling aperture also impacted by larger CK rise/fall time**

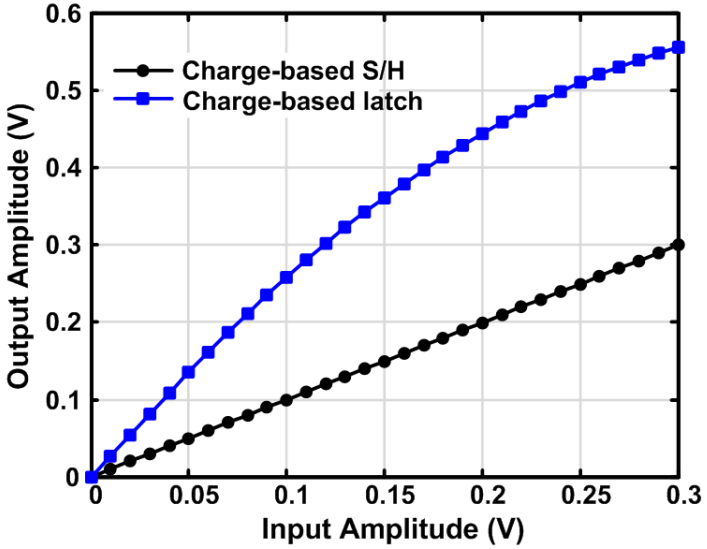
Proposed Charge-Based S/H



- Similar to proposed charge-based latch
- Cascode device reduces V_{CM} drop
- Shorting PMOS removes residual ISI at cascode node

Charge-Based S/H & Latch Performance





Sampling aperture:

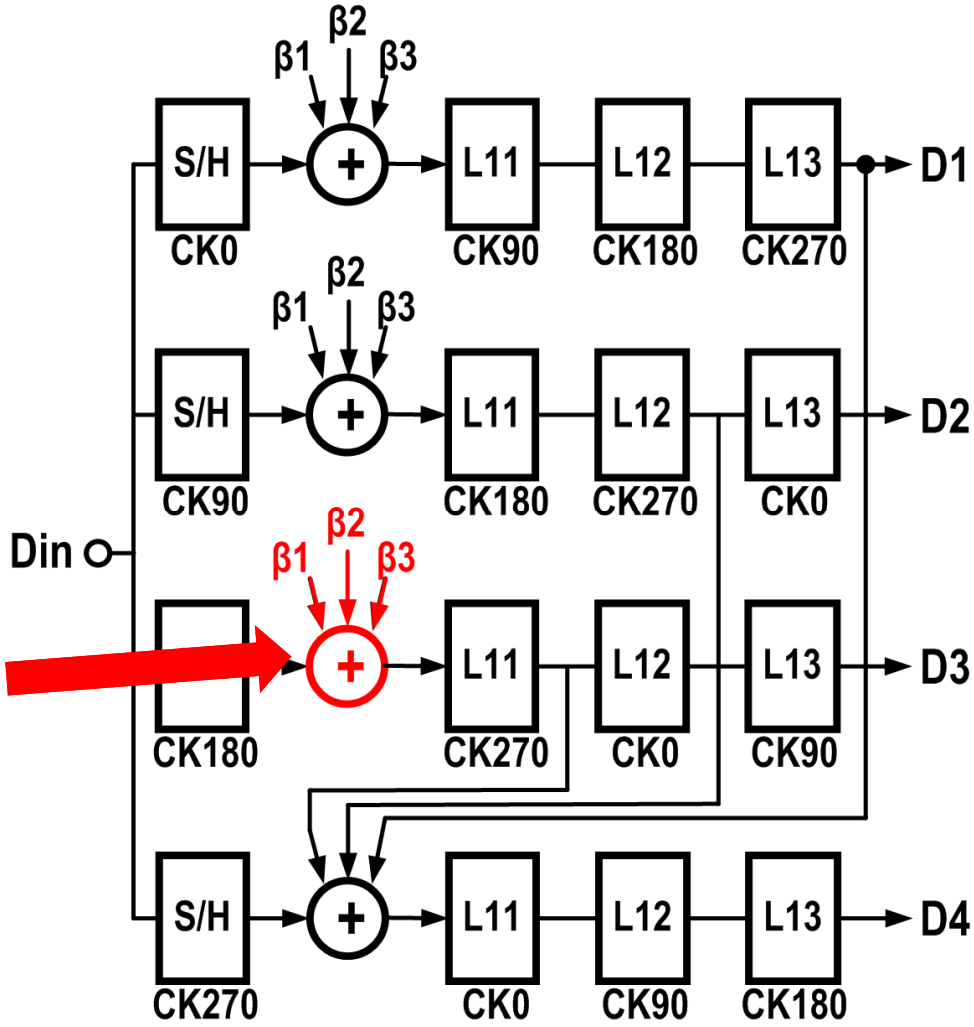
- ~17ps (post-layout)
- < 1UI at 16Gb/s

Gain:

- S/H gain set to 1, preserving linear range of proceeding summer
- Latch gain set to ~2

Low-V_{DD} DFE Design Challenges

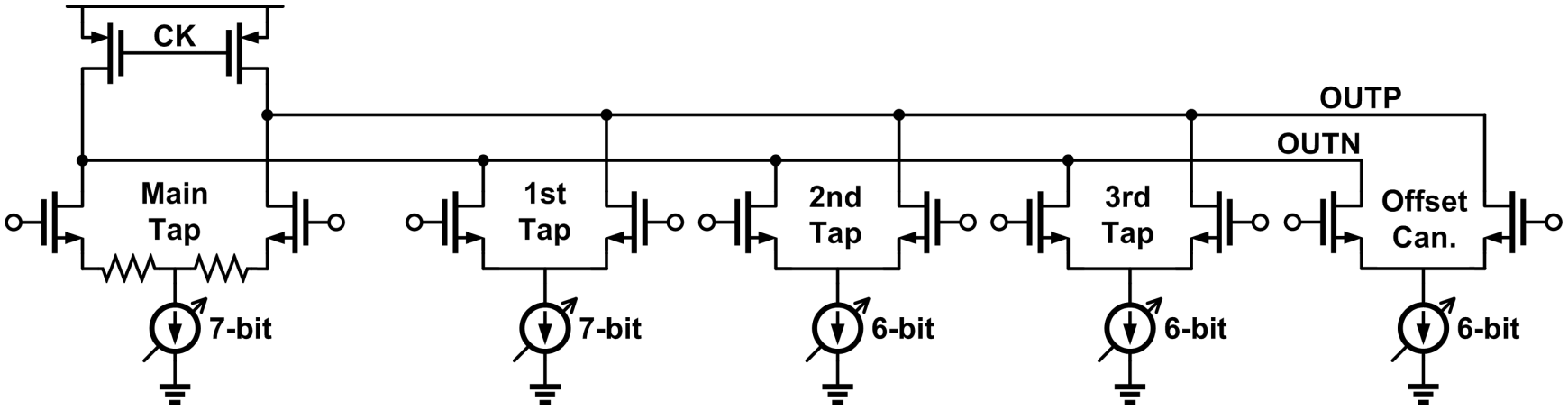
- Latch
- S/H
- Summer
  - Dynamic range and linearity degradation



Design of Integrating Summer

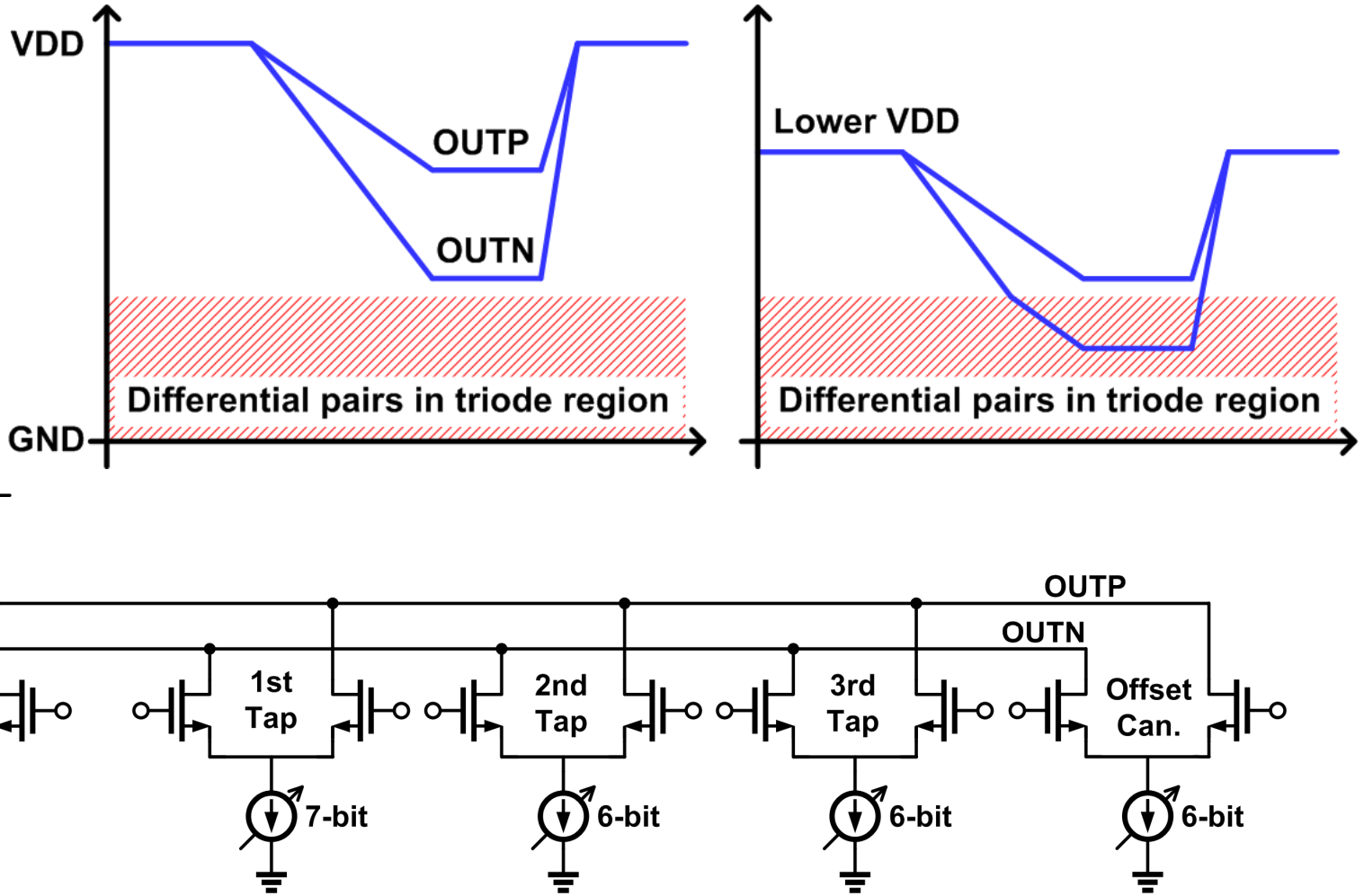
- Integrating summer* offers better energy-efficiency than a continuous-time summer
- V* of 1st-3rd differential pairs lowered, reducing the required latch output swing for the feedback taps

* Park, ISSCC 2007



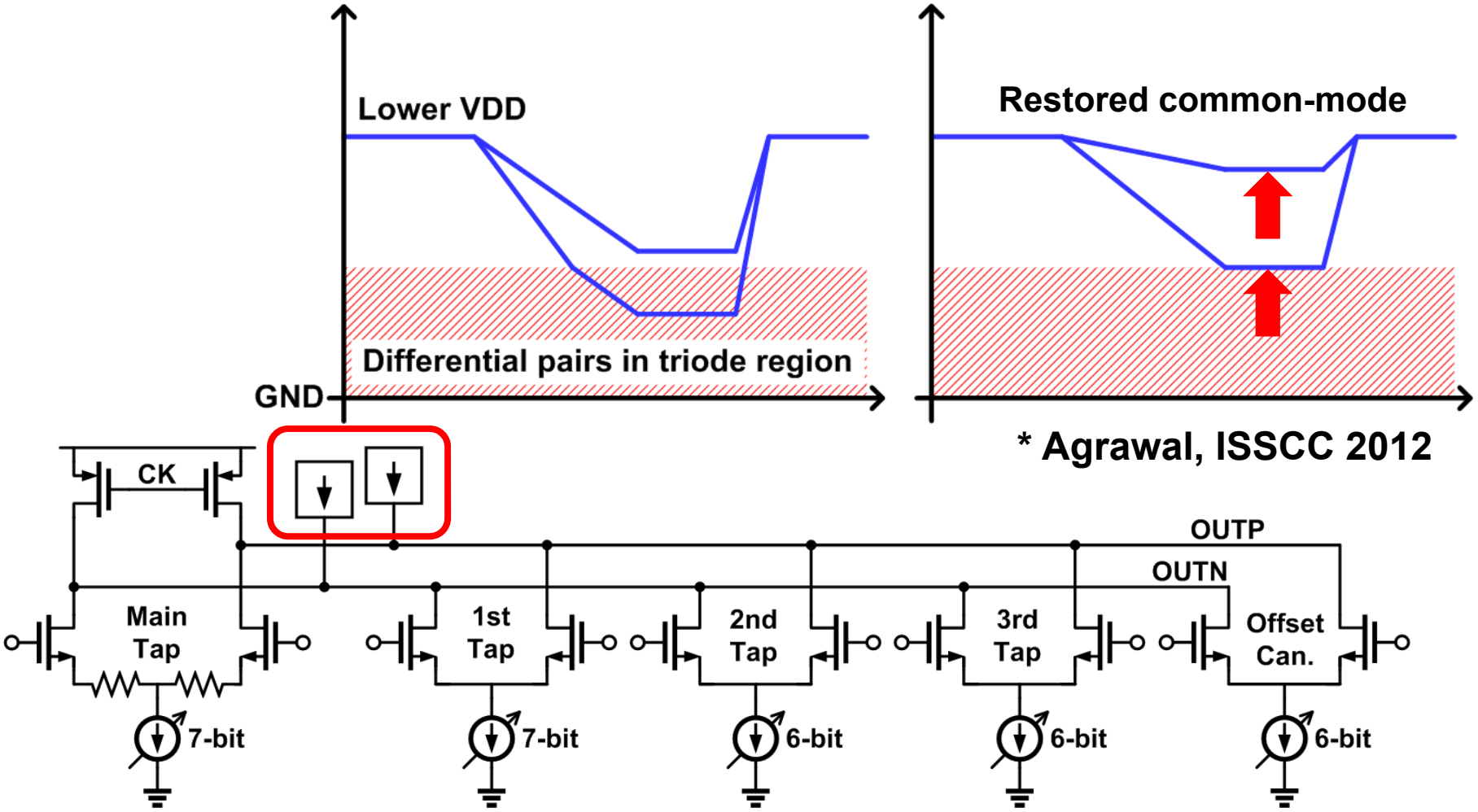
Summer Headroom Issue at Low-V_{DD}

Reduced headroom at low VDD degrades differential gain and linearity



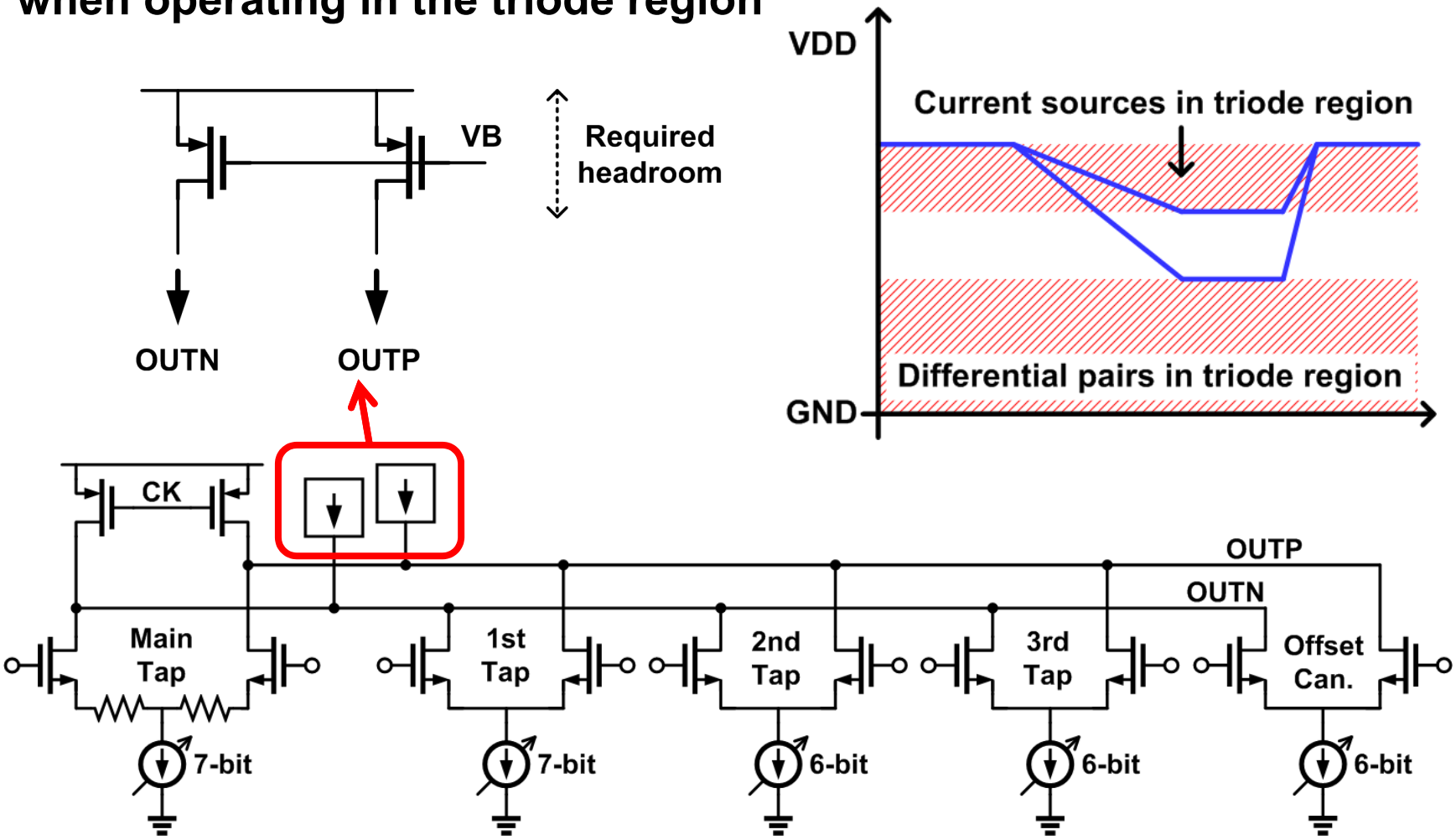
Summer Common-Mode Restoration

Common-mode restored by injecting current into summer output *

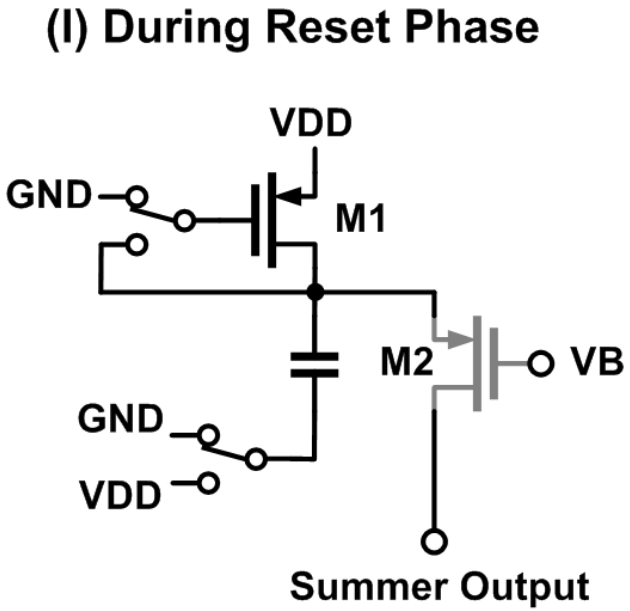


Problem with Current Injection

PMOS current sources will also degrade differential gain and linearity when operating in the triode region

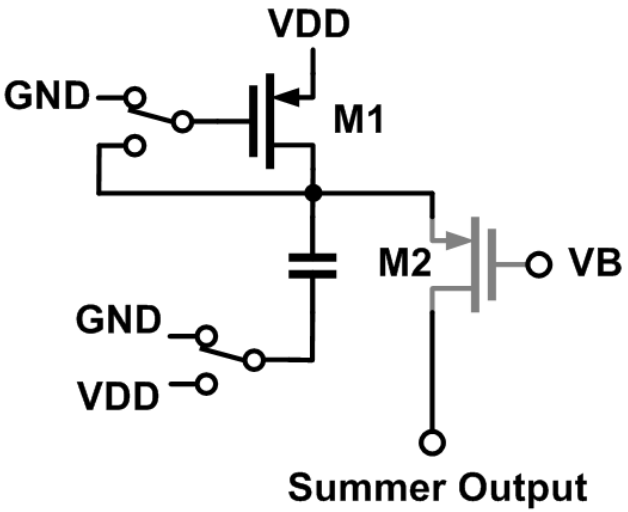


Proposed Bootstrapped Current Source



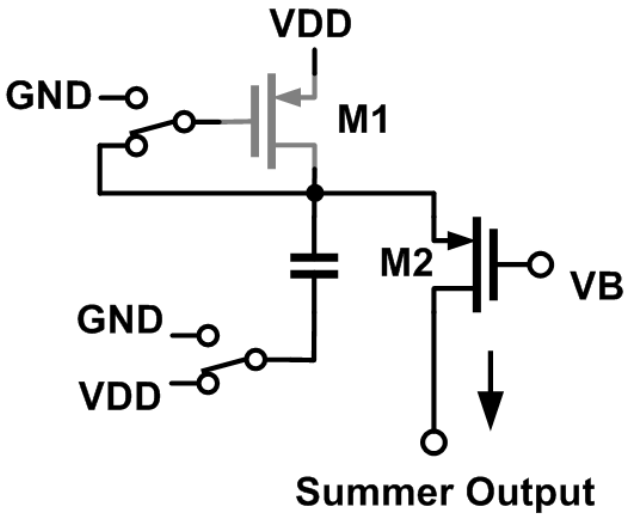
Proposed Bootstrapped Current Source

(I) During Reset Phase



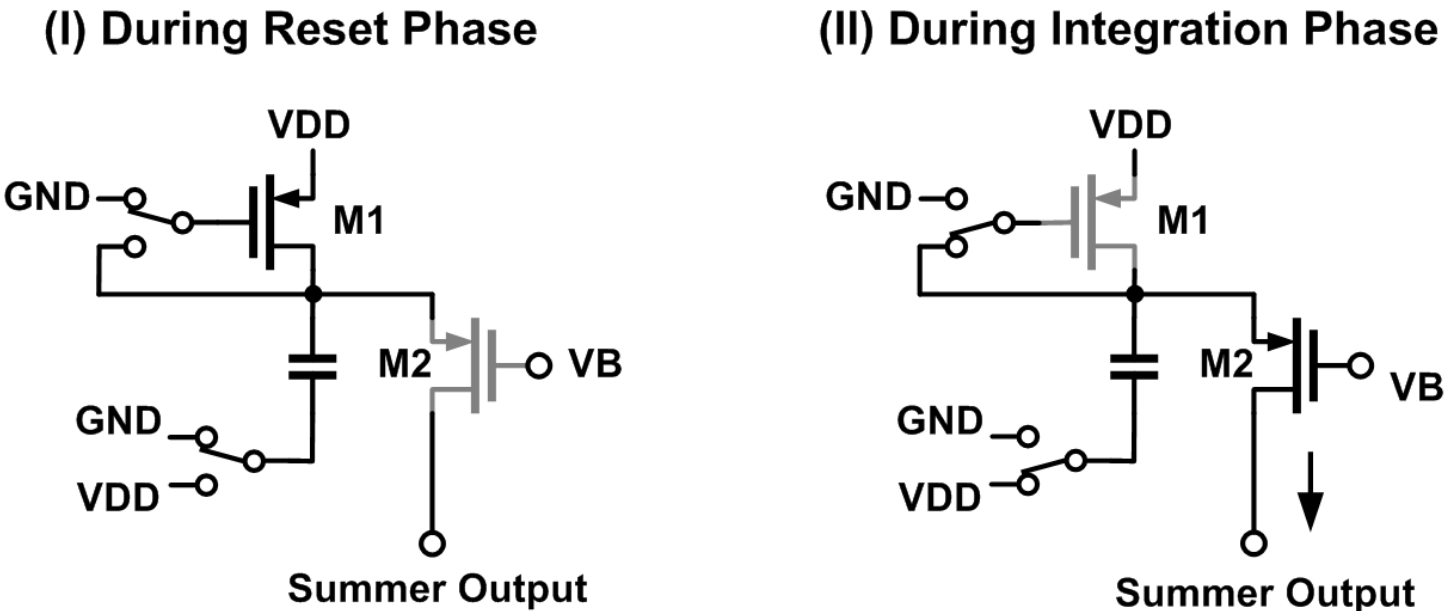
Charge capacitor during summer reset

(II) During Integration Phase



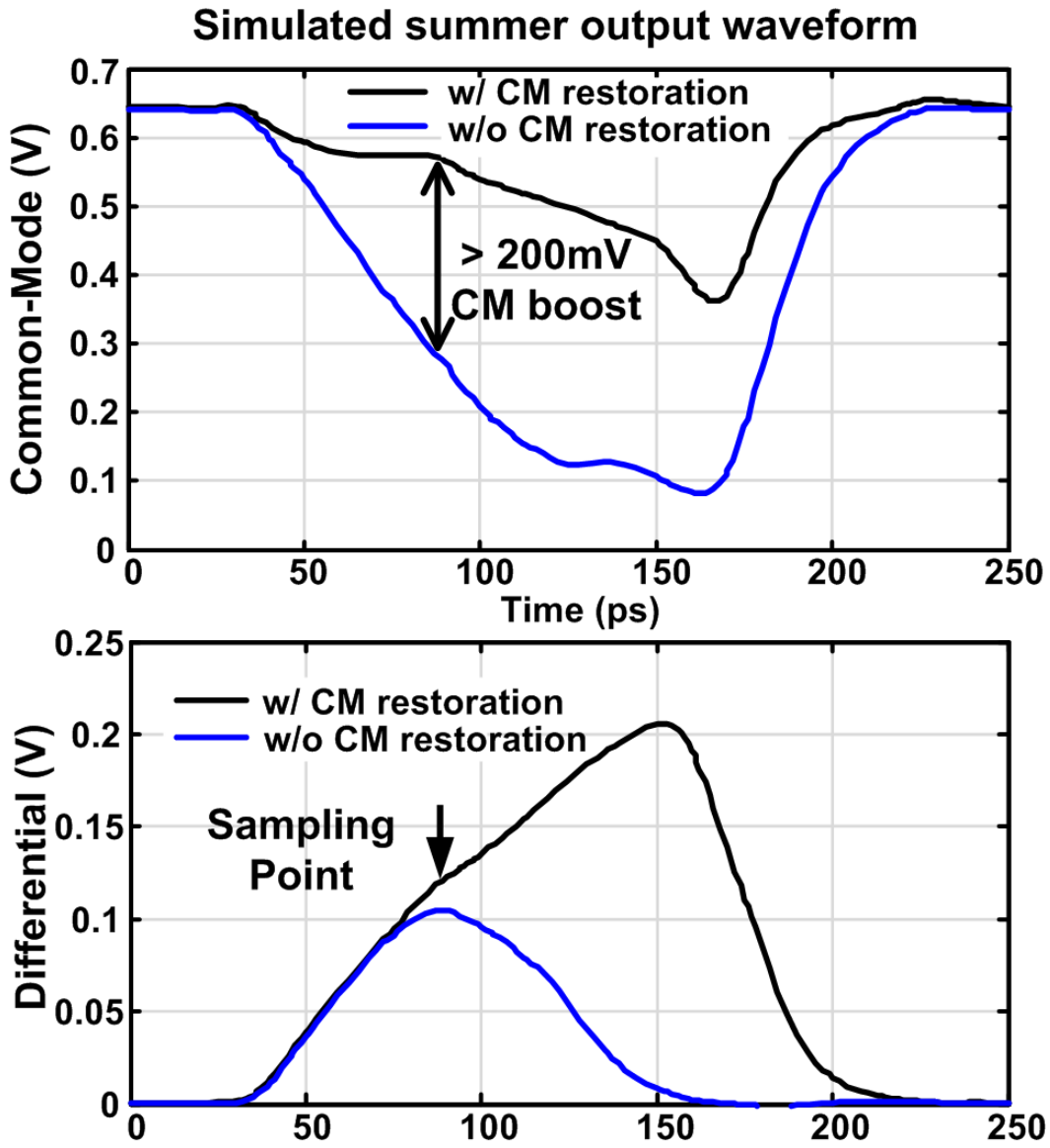
Bootstrap and discharge capacitor during summer integration

Proposed Bootstrapped Current Source

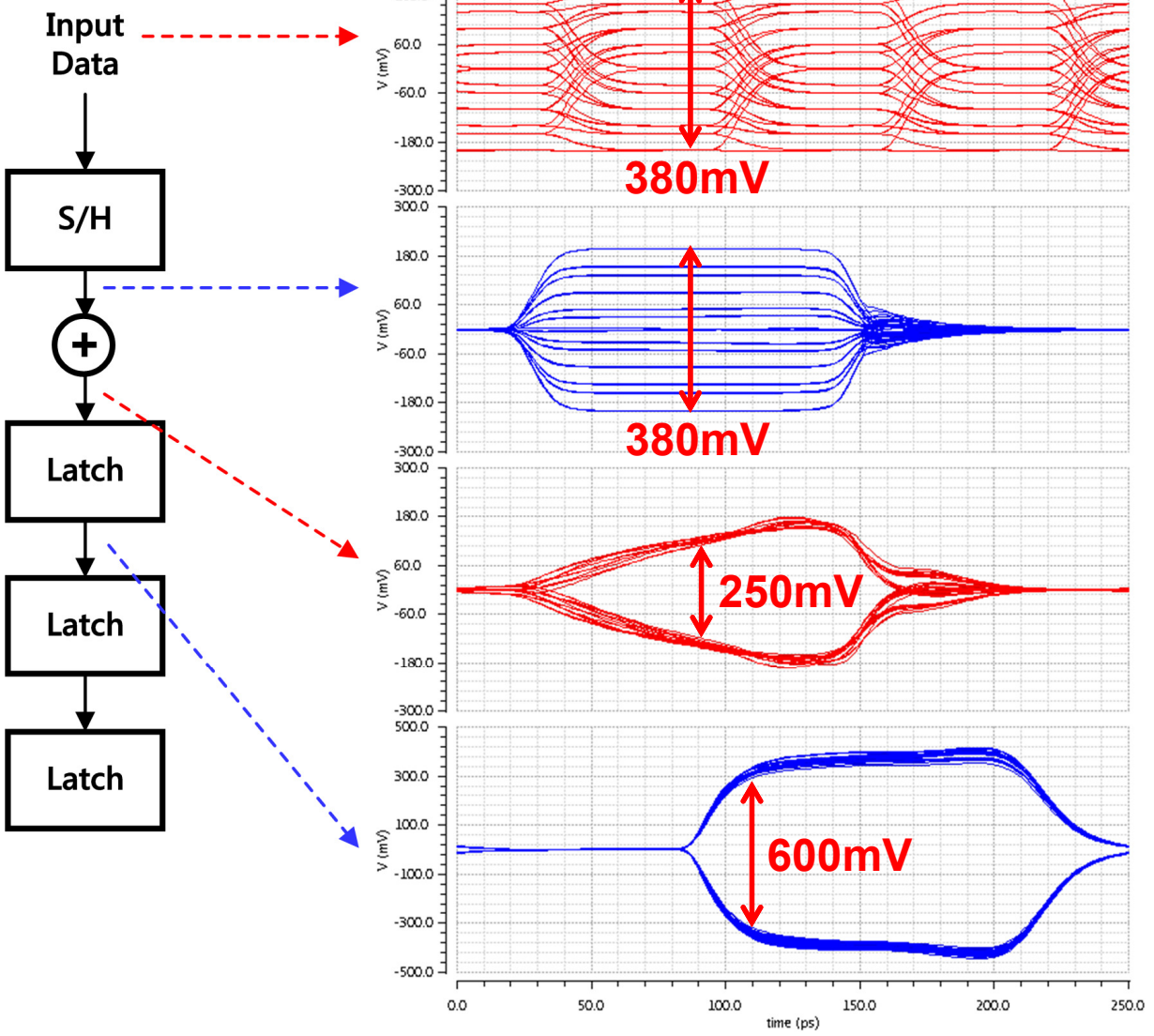


- Minimum degradation of gain and linearity
  - M2 kept in saturation for high output impedance
- Minimum area overhead to reduce parasitic loading
  - Adds 32 μm^2 to each summer

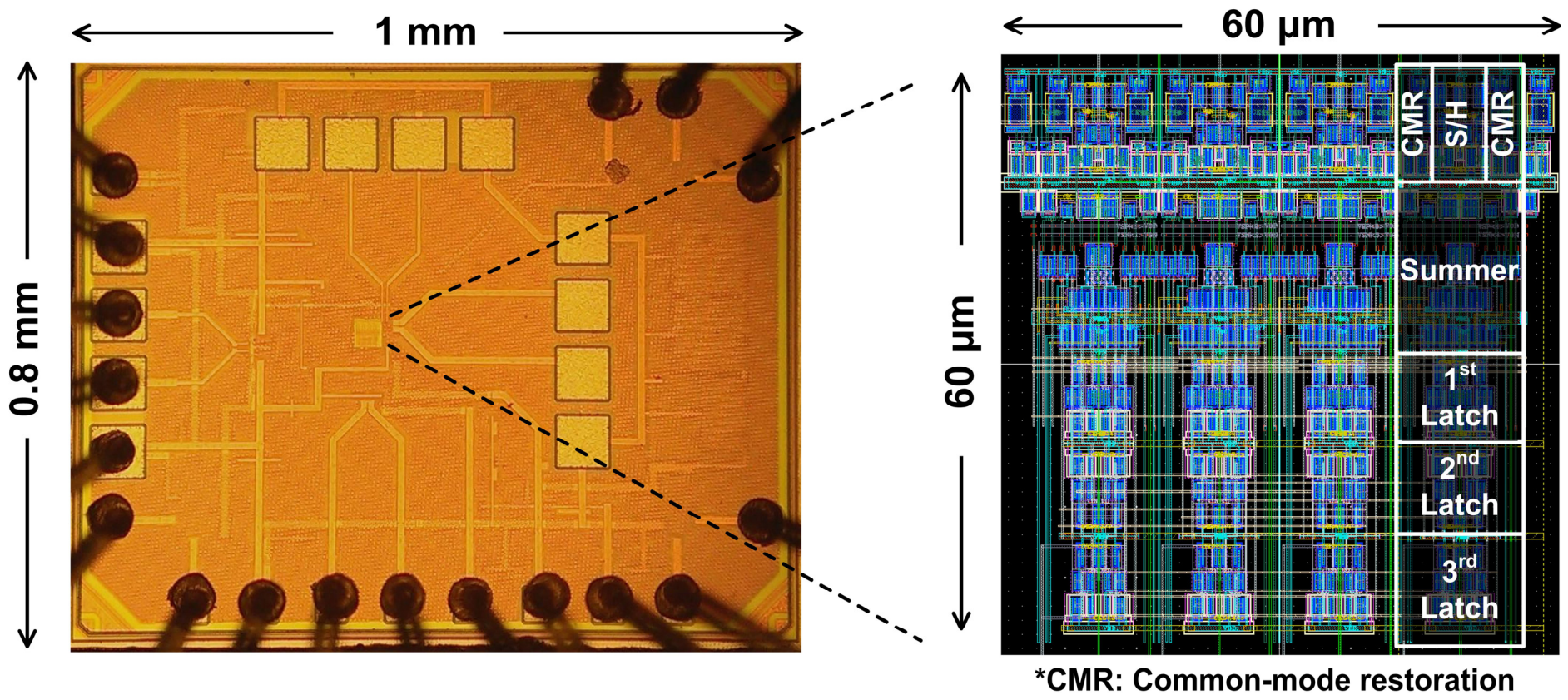
Summer Common-Mode Restoration



Simulated DFE Waveforms at 16Gb/s



Die Micrograph



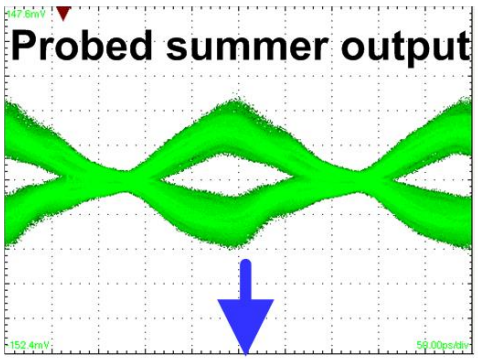
- Test chip fabricated in 65nm GP

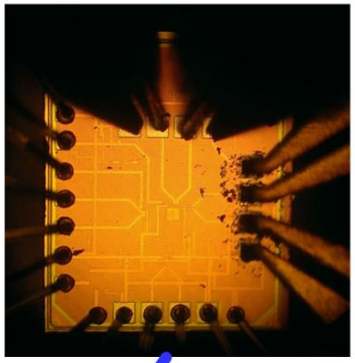
→ DFE core area = 60um x 60um

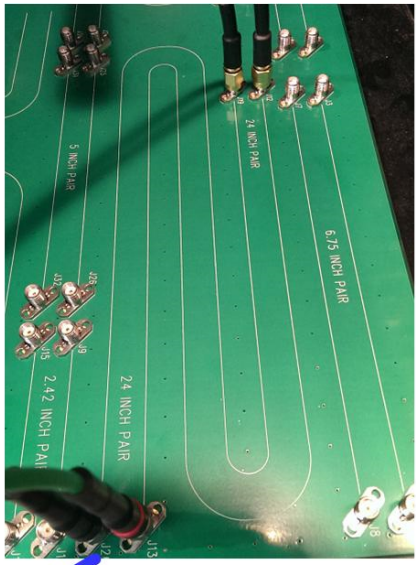
Outline

- Motivation for low-V_{DD} DFE
- Architecture of proposed DFE
- Low-V_{DD} DFE design challenges
- Measurement results
- Conclusions

Test Setup







Oscillo-scope

Probe

DUT

MUX

DFE

DIV/2

Probe

Test Channel

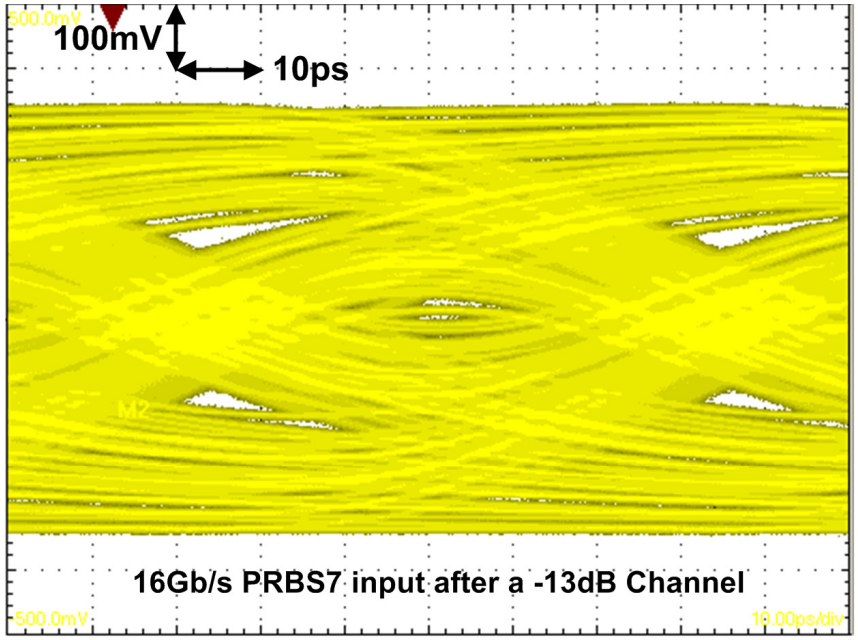
16Gb/s Data

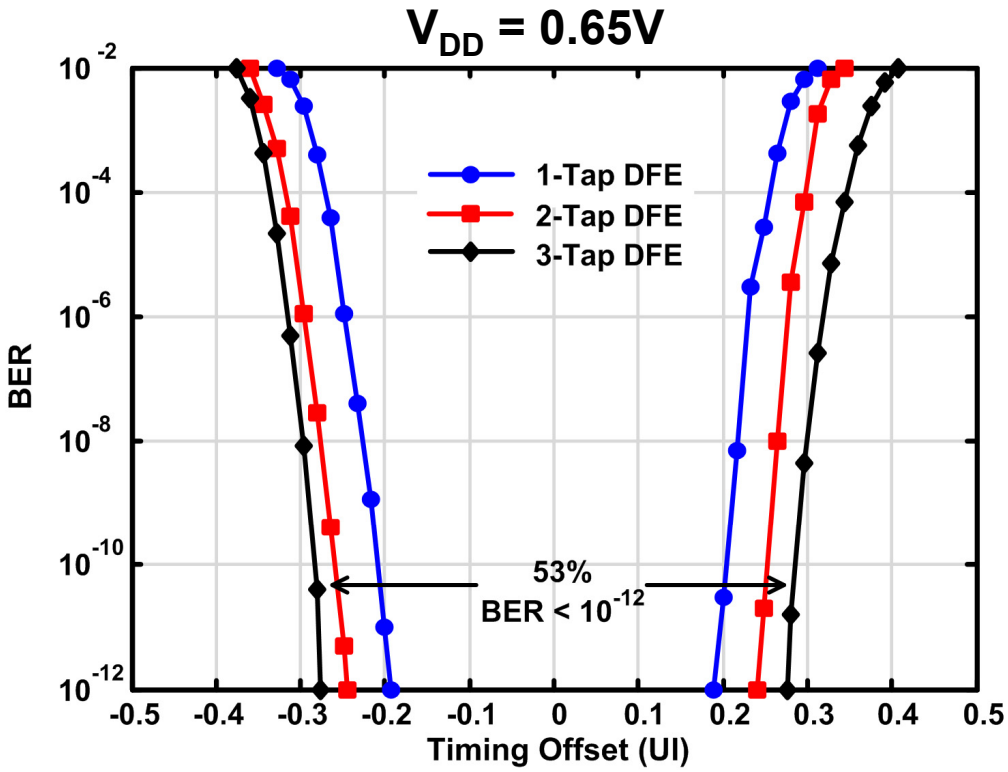
8GHz Clock

BERT

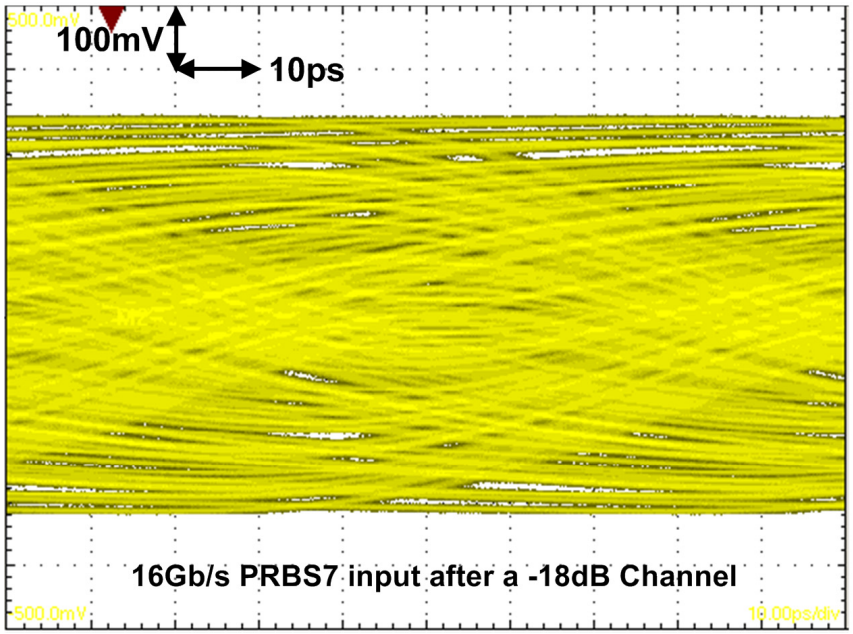
4Gb/s Recovered Data

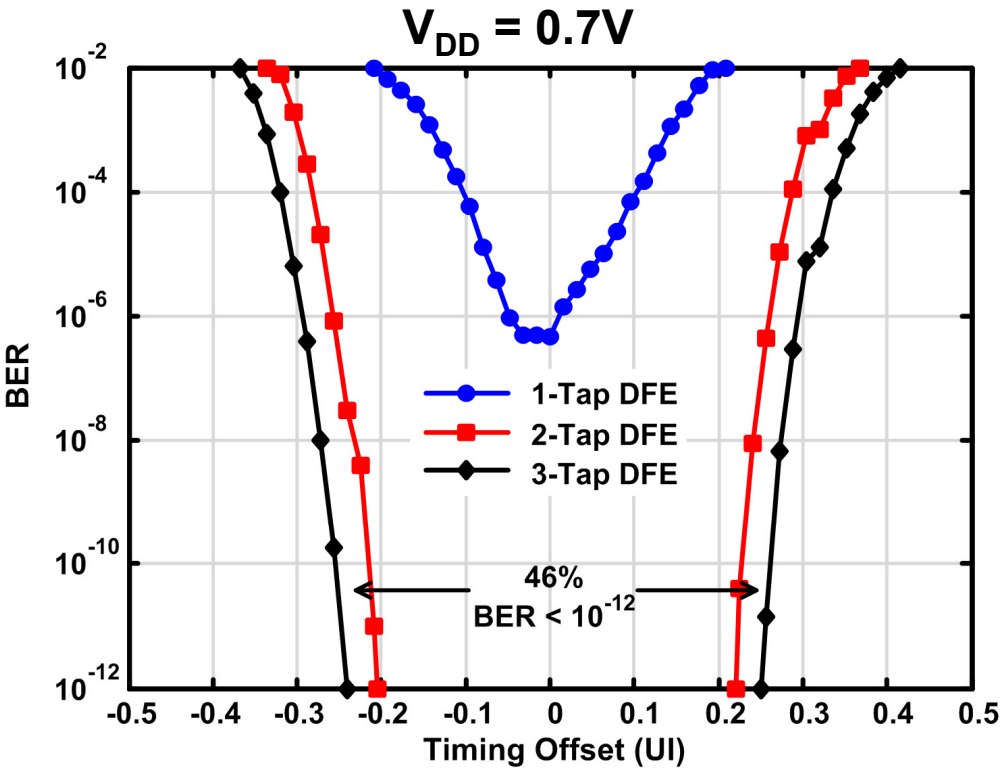
Measured BER Bathtub with -13dB Channel



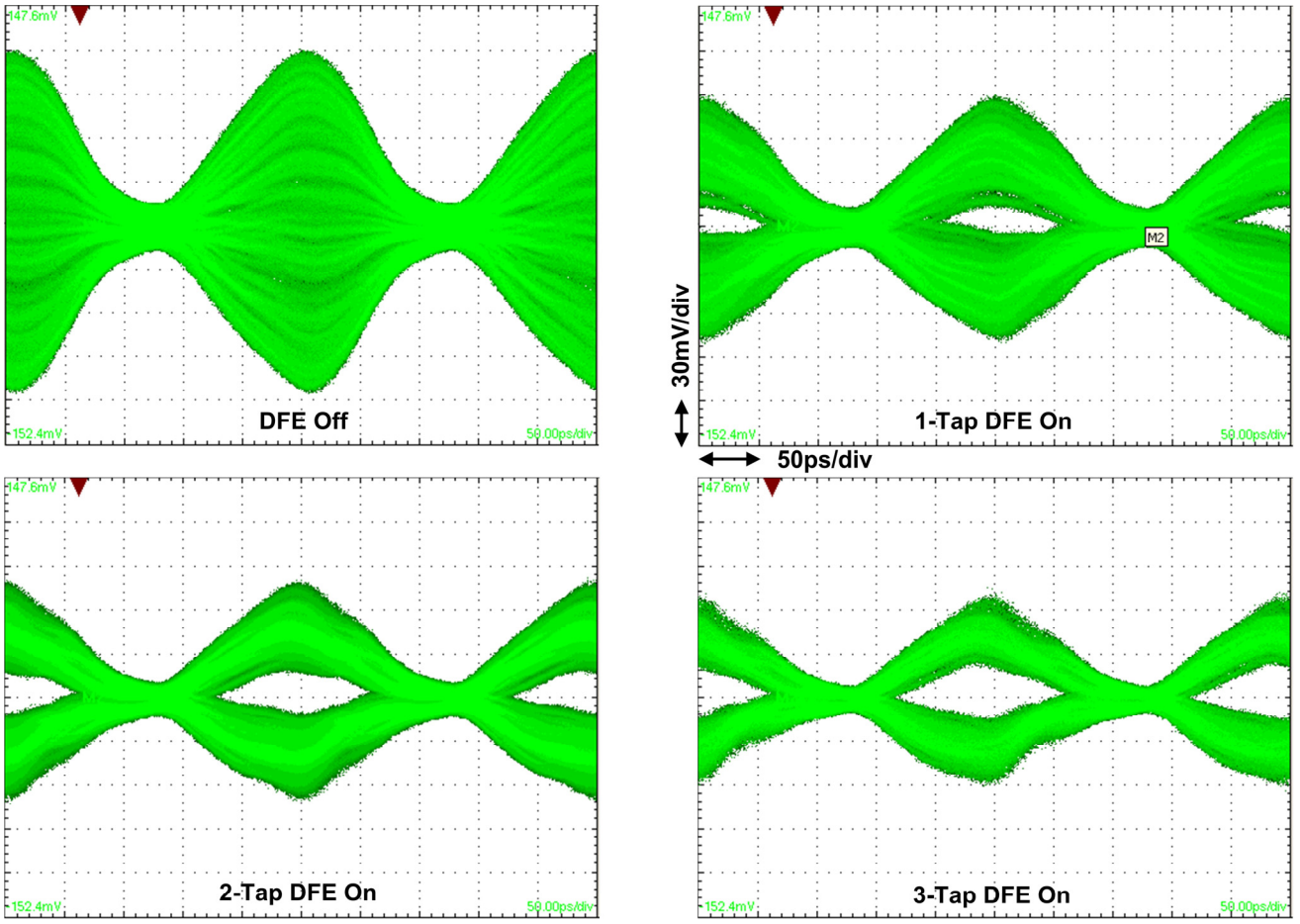


Measured BER Bathtub with -18dB Channel





Measured Internal Eye Diagram of Summer

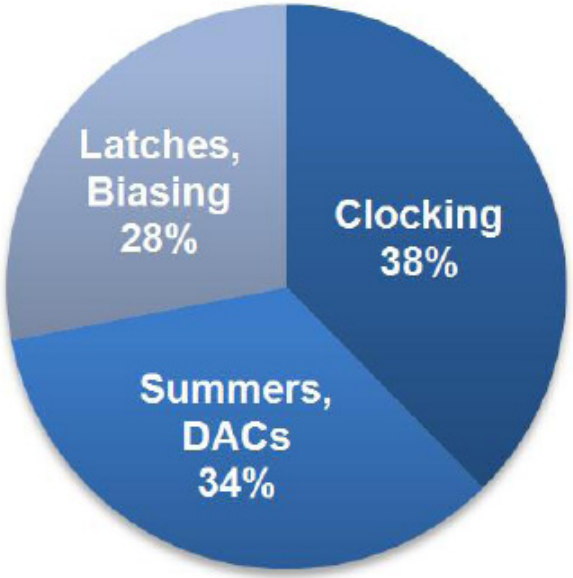


DFE successfully removes ISI from -18dB channel

Power Breakdown

Component	Power (mW)
Summers and DACs	1.4
Latches and biasing	1.1
Clocking	1.5
Total	4

0.7V 16Gb/s



*** Does not include power of CML clock divider and CML-CMOS converter**

Performance Summary

References	M. Nazari ISSCC 2011	J. Proesel VLSI 2011	K. Kaviani ISSCC 2012	This Work	
Data Rate (Gb/s)	15	20	16	16	
Process	45nm SOI	45nm SOI	40nm GP	65nm GP	
Equalization	2-tap DFE	CTLE + 1-tap DFE	Passive LE + 1-tap DFE	3-tap DFE	
Clocking	Half Rate	Half Rate	Half Rate	Quarter Rate	
Supply (V)	1.2	1.2	1.0	0.65	0.7
Channel Loss (dB)	14.5	26.3	15	13	18
Timing Margin	34% BER < 10^{-8}	26% BER < 10^{-12}	>25% BER < 10^{-12}	53% BER < 10^{-12}	46% BER < 10^{-12}
Power (mW) (Including Clocking)	7.5	13.2	9.25	3.3	4
Energy Efficiency (pJ/b)	0.50	0.66	0.59	0.21	0.25

Conclusion

- A low-V_{DD}, 16Gb/s, 3-tap DFE is presented in 65nm-CMOS
- Several techniques proposed to overcome performance degradation at 0.65~0.7V
  - Charge-based latch and S/H
  - Summer common-mode restoration
- The DFE achieves 0.21pJ/b at 0.65V and 0.25pJ/b at 0.7V
- The proposed architecture is suitable for higher data-rates, and application in advanced process nodes

Acknowledgement

- Department of Energy Early CAREER program
- Intel Labs Wireline Signaling Program
- Semiconductor Research Corporation TxACE (Grant #1836.060)
- John Calvin of Tektronix; Elad Alon, Yue Lu of UC Berkeley; Jiao Cheng, Matthew Brown of OSU; Kangmin Hu of Broadcom

A 5.67mW 9Gb/s DLL-Based Reference-less CDR with Pattern-Dependent Clock-Embedded Signaling for Intra-Panel Interface

Dong Hoon Baek[1,2], Byungsub Kim[1], Hong-June Park[1], Jae-Yoon Sim[1]

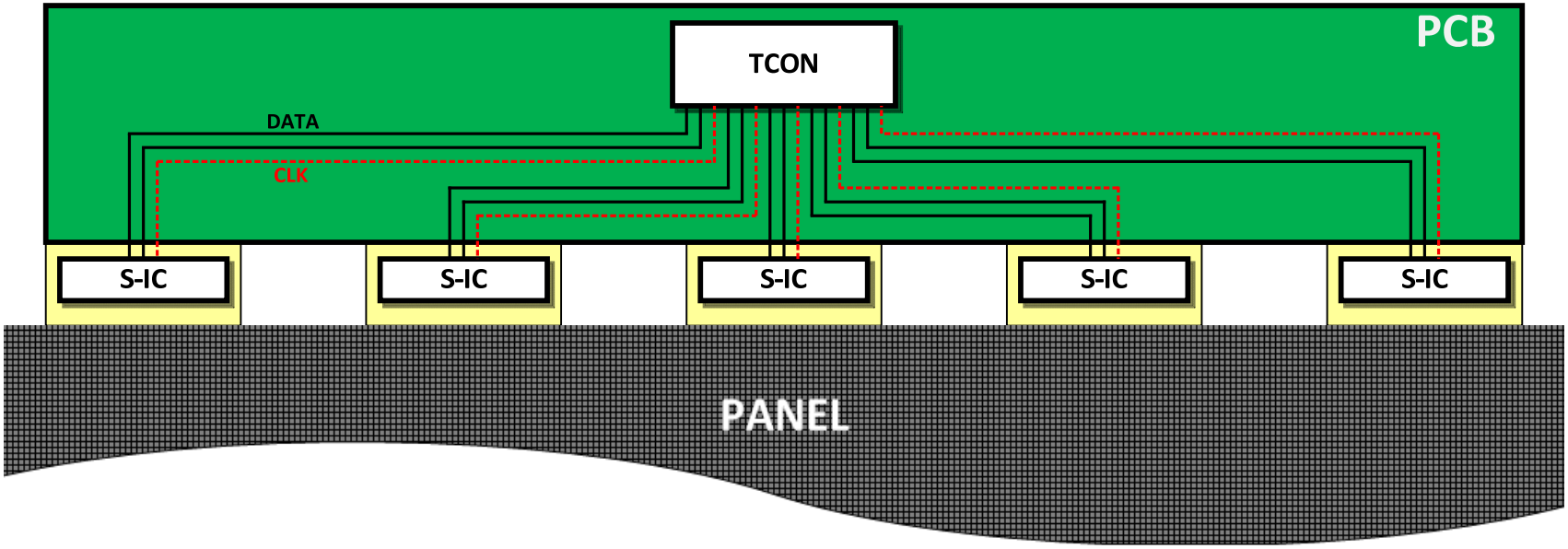
[1]POSTECH, Pohang, Korea
[2]Samsung Electronics, Yongin, Korea

Outline

- **Introduction**
  - Background of Intra-Panel Interface
  - Previous Approaches of Clock-Embedded Signaling
- **Proposed Scheme**
  - Pattern-Dependent Clock-Embedded Signaling
  - Building block & Simulation
- **Implementation Results**
- **Conclusion**

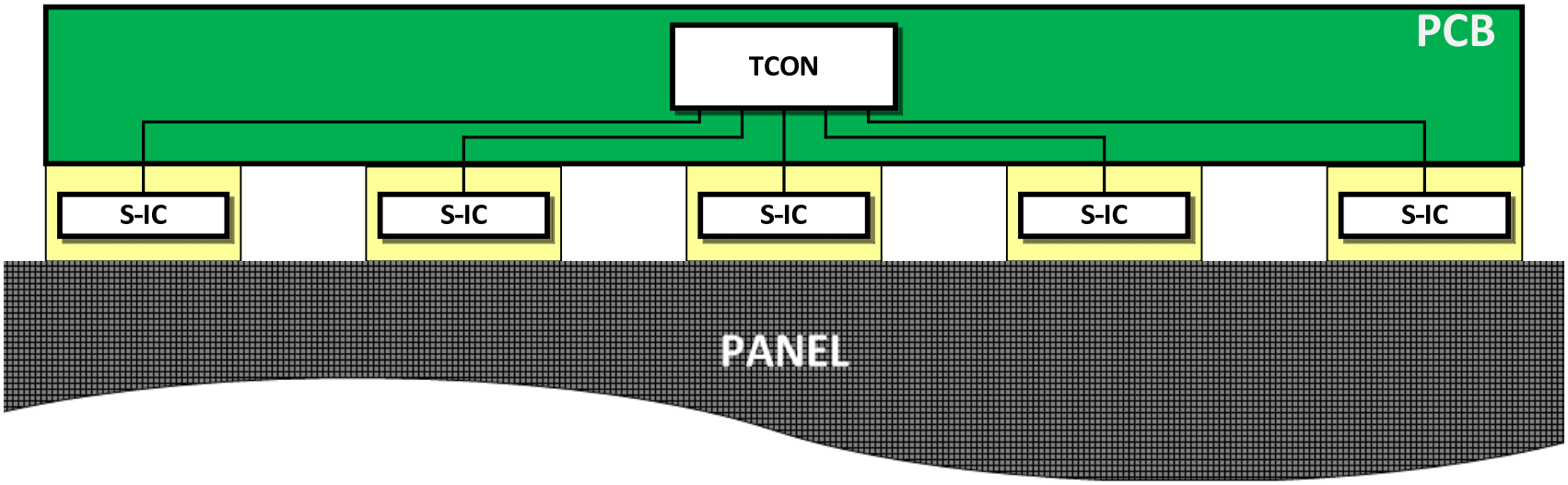
Intra-Panel Interface

- Interface between timing controller (TCON) and multiple source drivers(S-IC) on display panel
- Panel interface architecture : Separated CLK
  - Skew problem between DATA and CLK lanes
  - Large EMI



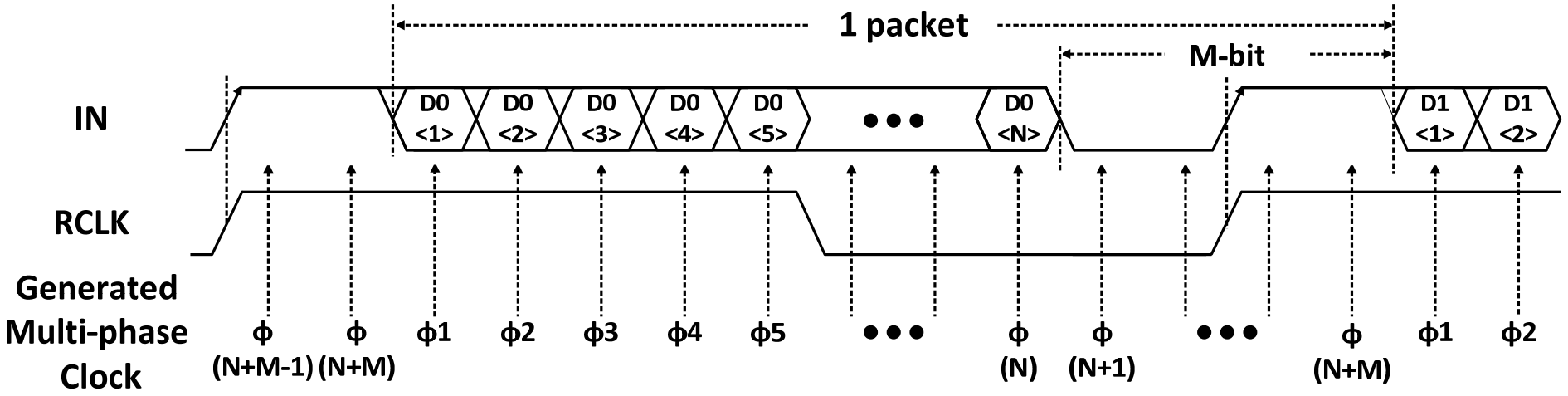
Intra-Panel Interface

- Interface between timing controller (TCON) and multiple source drivers(S-IC) on display panel
- Panel interface architecture : Embedded CLK
  - No skew
  - Reduced EMI
  - Narrow PCB (Bezel): cost reduction and slim design



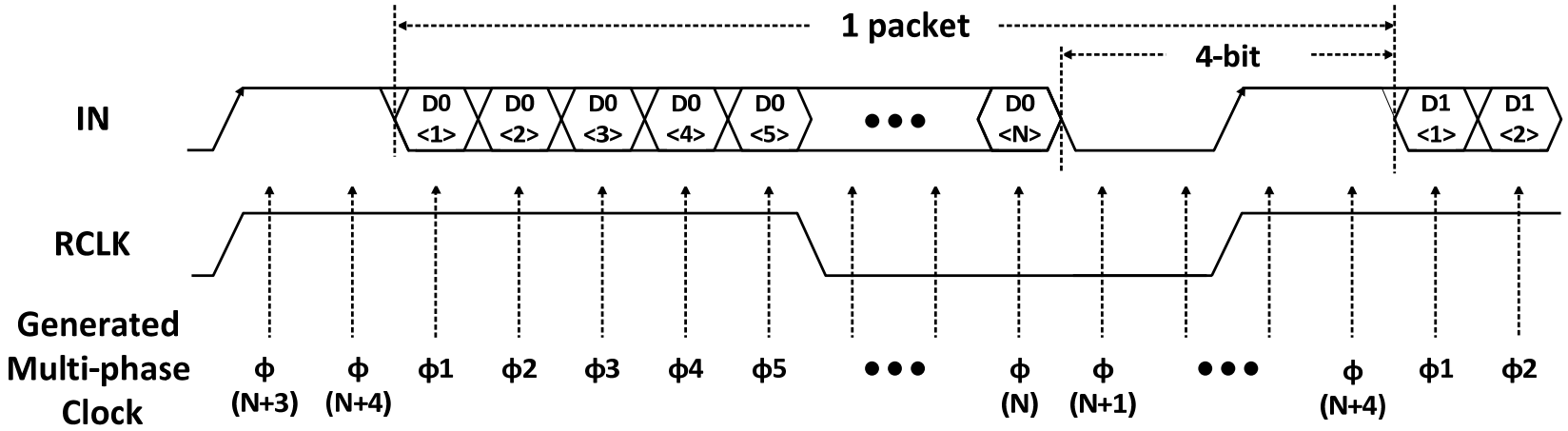
Clock Embedded Signaling (CES)

- 1-packet: N-bit display data + M-bit overhead
- Clock Recovery (RCLK): By extraction of transition information in M-bit
- Data Recovery: Sampling with multi-phase DLL
- M is chosen according to ISI and bandwidth requirements

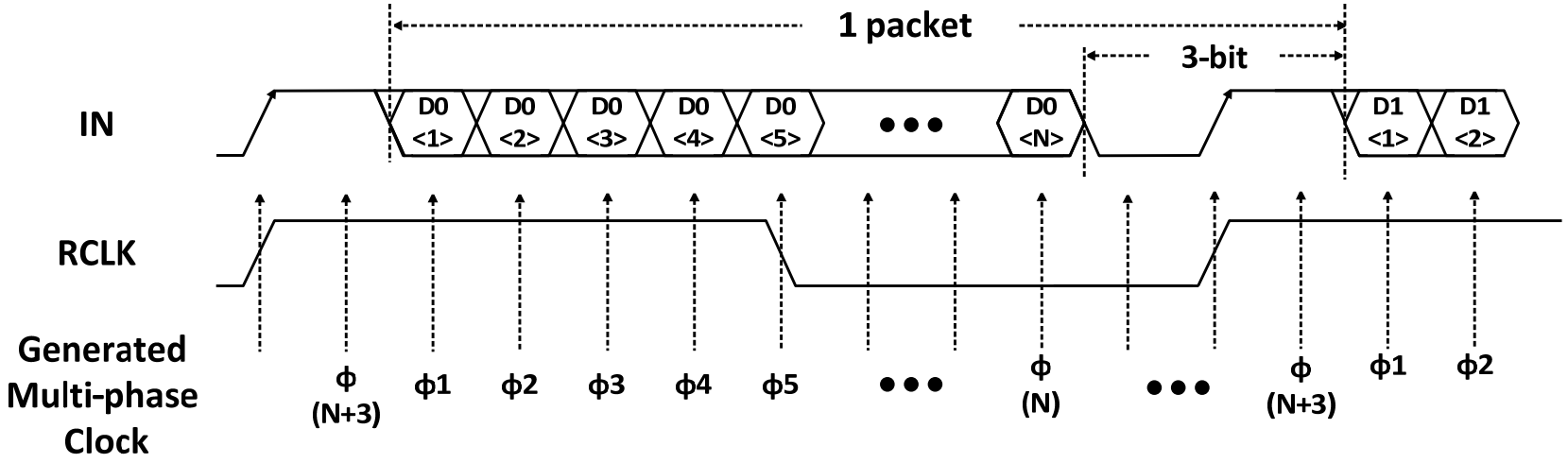


Previous Approaches of CES

- **H.-K.Jeon [SID2009]: 2x VCDL cells**

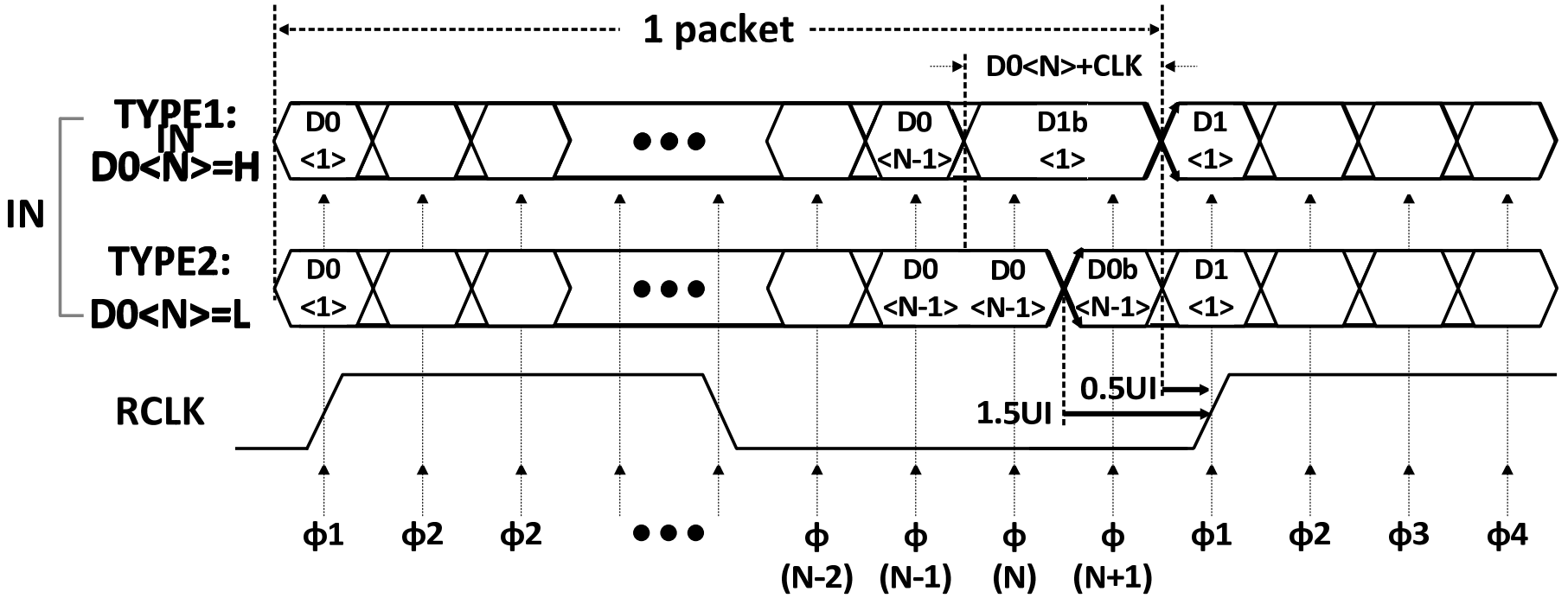


- **S.Jang [ISSCC2011]: 2x operating frequency @Tx**



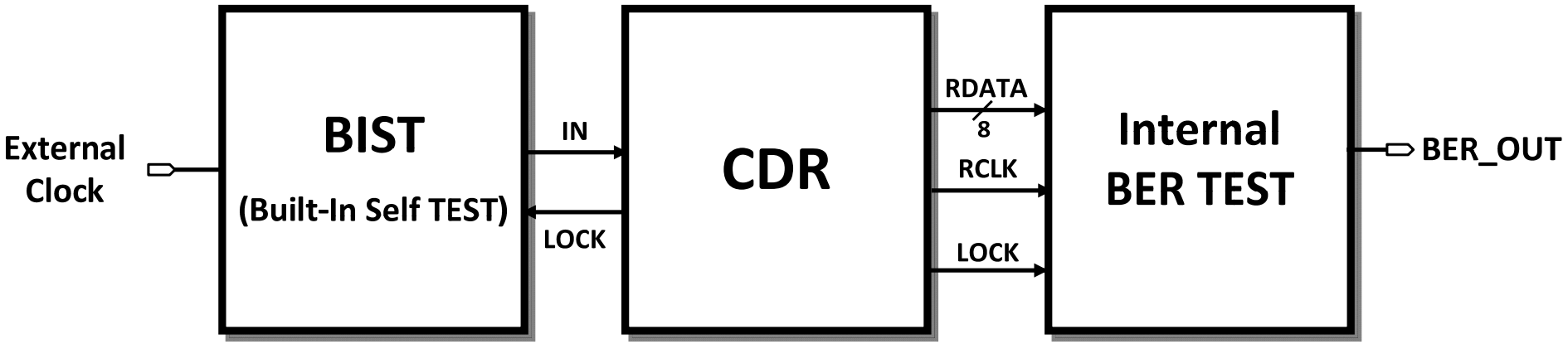
Proposed CES : Pattern Dependent

- There are 2 types of packet depending on MSB
  - MSB=H : TYPE1, MSB=L : TYPE2
- At least 2bit run-length before reference transition
- Effective overhead = 1bit
- EMI as good as PRBS data → EMI eliminated



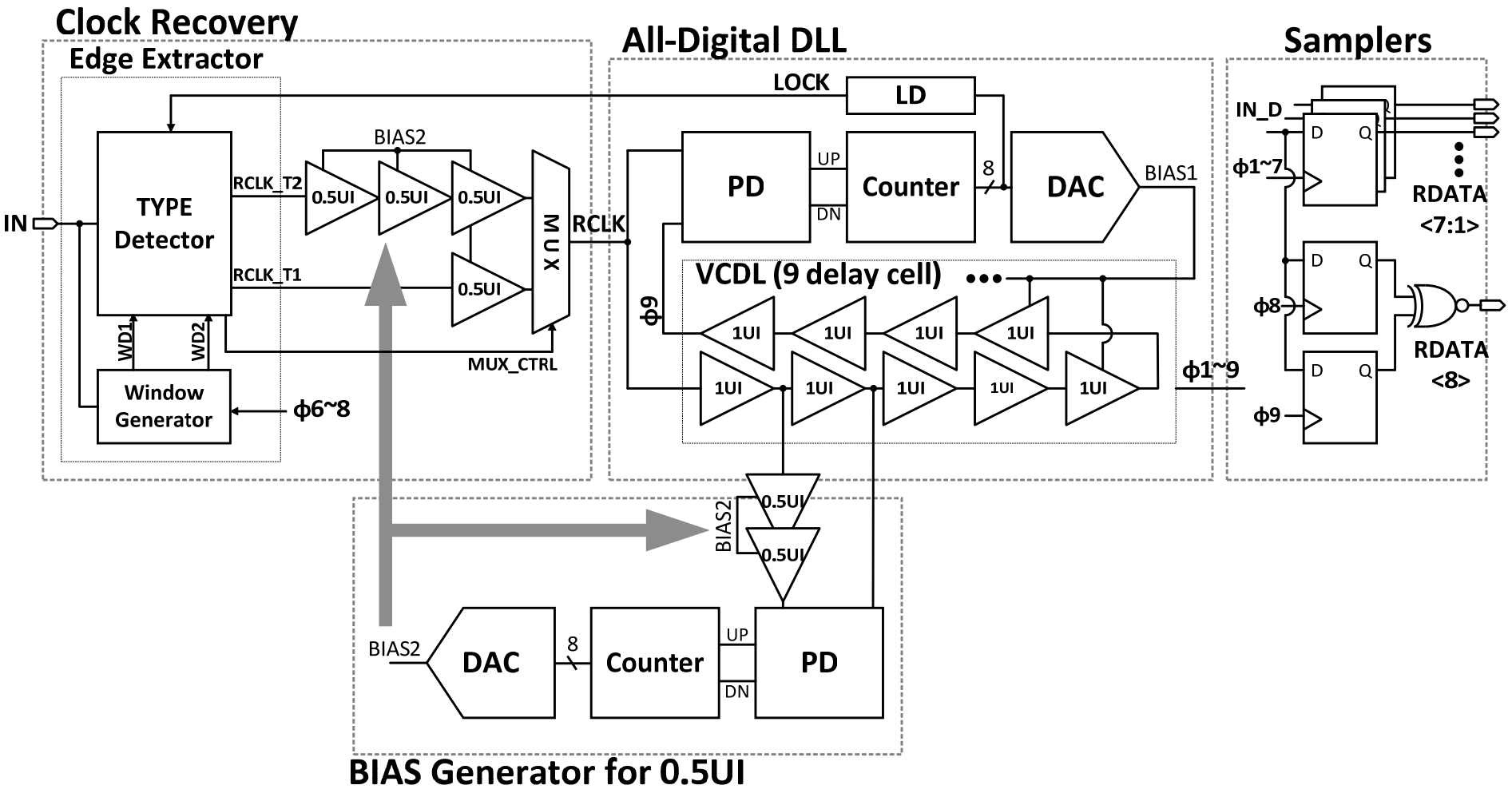
Design for On-Chip BER Test

- BIST: Proposed CES pattern generator
- Internal BER TEST: On-chip BER tester



DLL-Based CDR

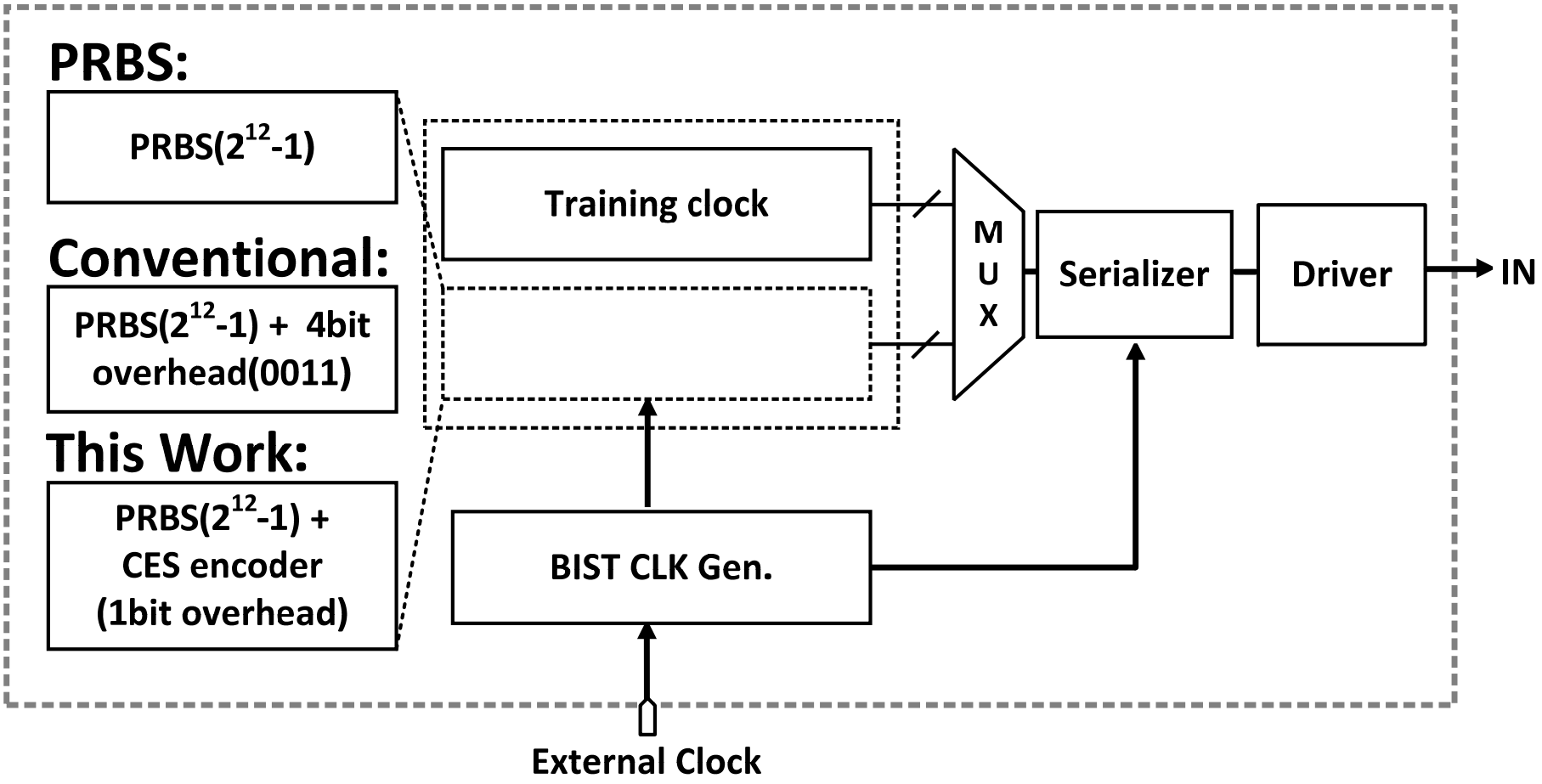
– Dual-loop architecture to generate 0.5-UI delay



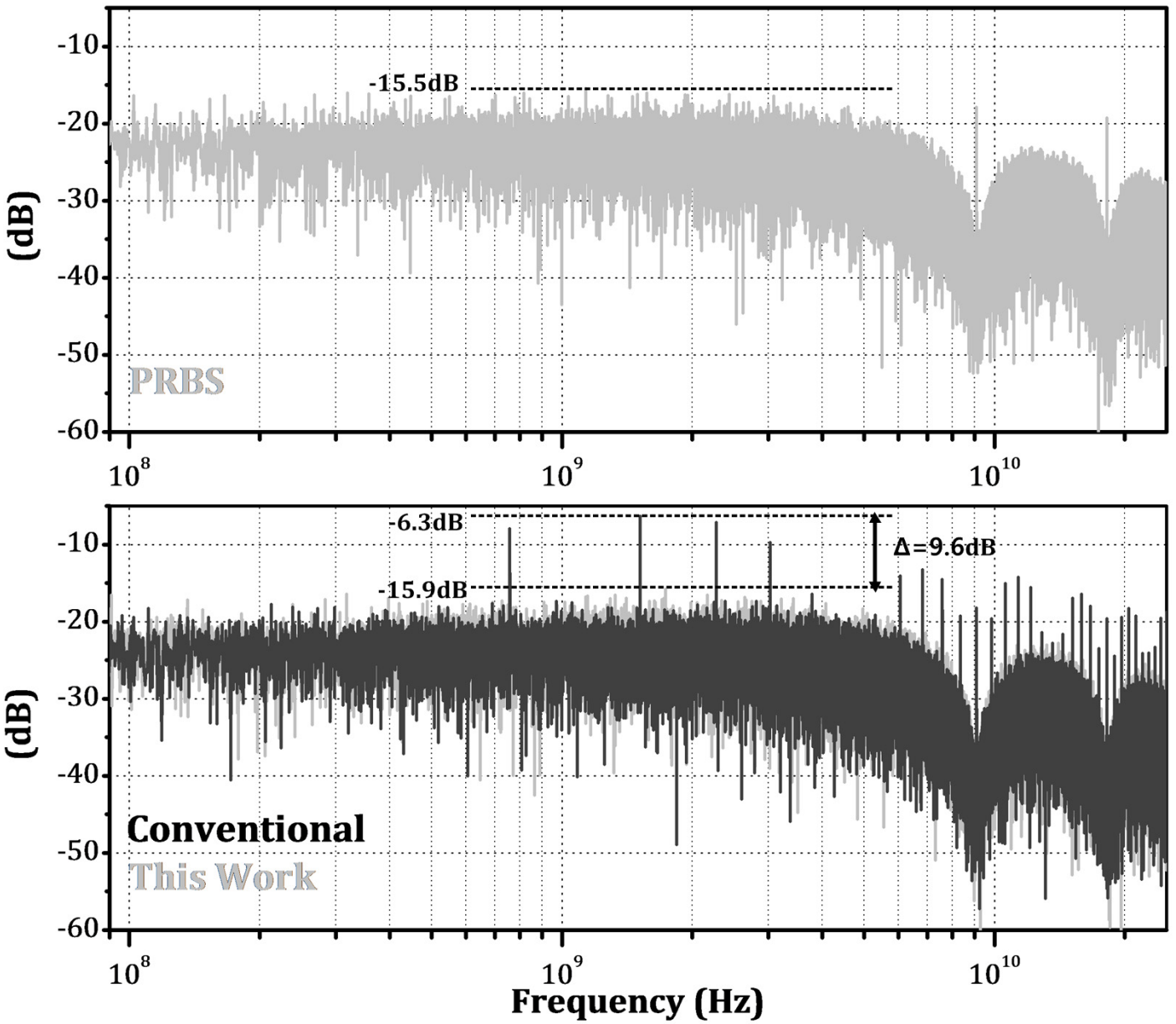
Comparison with Simulation

– EMI comparison

• PRBS, Conventional CES, Proposed CES

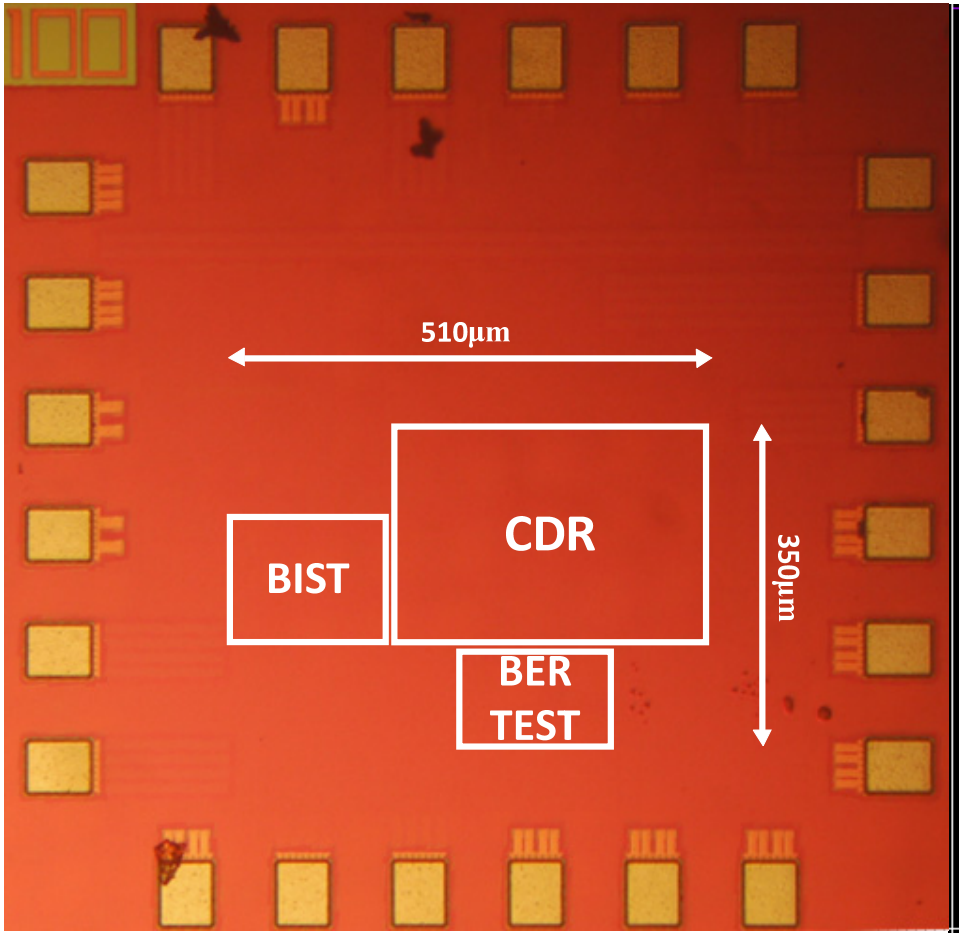


Simulated Spectra at 9Gb/s

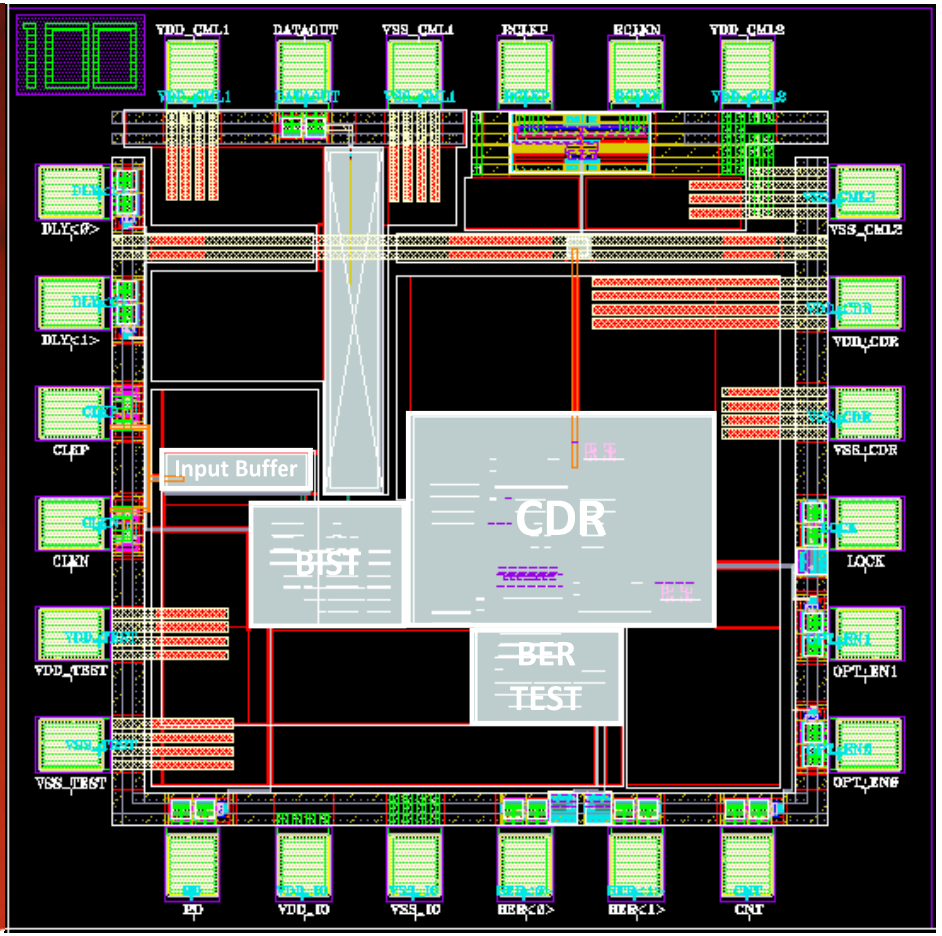


Chip Implementation (65nm CMOS)

- Die photo

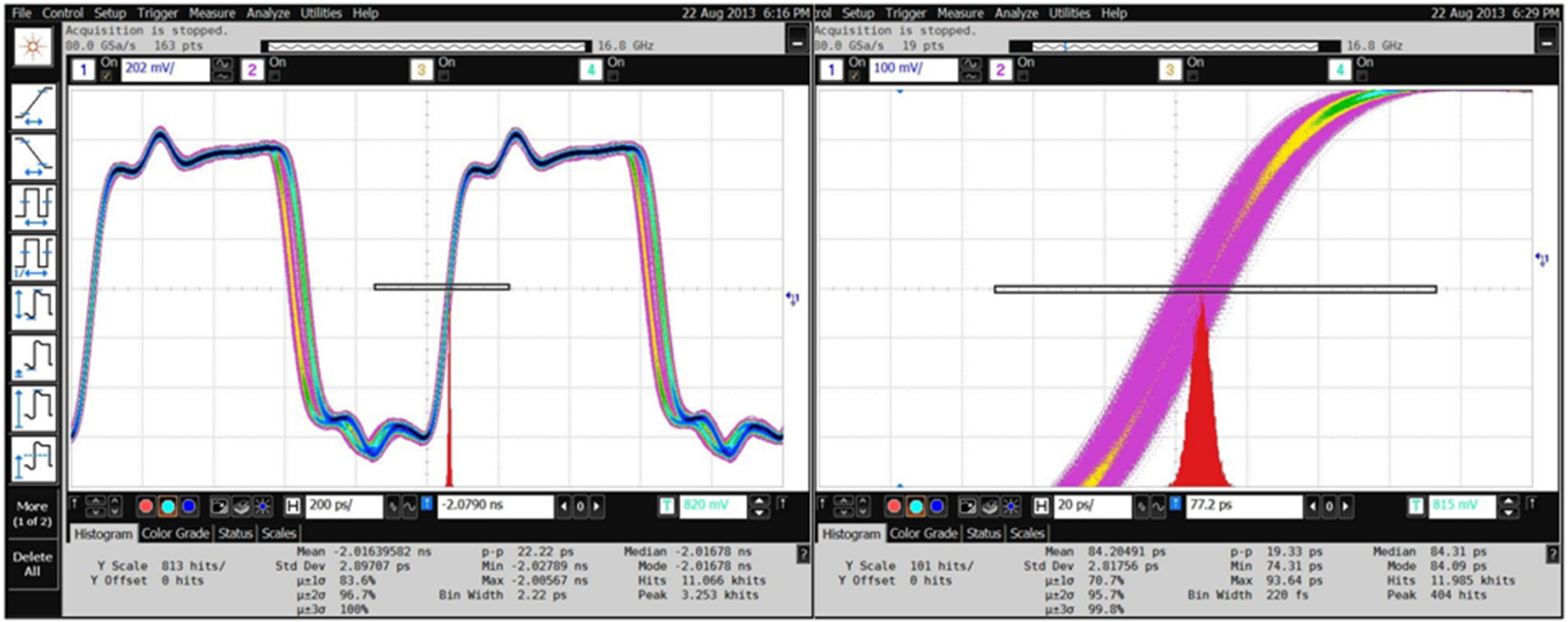


- Layout



Measurements

- **Recovered clock and jitter histogram @ 9Gb/s**
  - **RMS jitter: 2.82ps, peak-to-peak jitter: 19.33ps**



Chip Summary

	ISSCC '09 [1]	TCAS-II 09 [2]	ISSCC '11 [4]	ESSCIRC '12 [5]	This work
Technology	0.25 µm	0.25 µm	0.13 µm	0.13 µm	65 nm
Supply Voltage	3.0 V	2.5 V	1.2 V	1.2 V	0.9 V
CDR Type	PLL	PLL	Analog DLL	Digital DLL	Digital DLL
Overhead in packet	4B5B coding	4bit	3bit	2bit	1bit
Data Rate (Gb/s)	1.25 ~ 3.0	0.14 ~ 1.82	1.36 ~ 3.0	~ 3.0	6.5 ~ 9.0
RMS jitter (ps)	11 @ 2Gb/s	14.96 @ 1.82Gb/s	5.85 @ 3Gb/s	4.8 @ 3Gb/s	2.82 @ 9Gb/s
Power efficiency (mW/Gb/s)	46.5	75.27*	1.93	2.24	0.63
Area (mm^2)	0.45	2*	0.064	0.076	0.057

* : IN/OUT buffers included

Conclusion

- **Pattern-dependent CES is proposed for intra-panel interface**
  - Clock embedded with 1b overhead
  - 2b run-length guaranteed before clock transition
  - Eliminate EMI issue

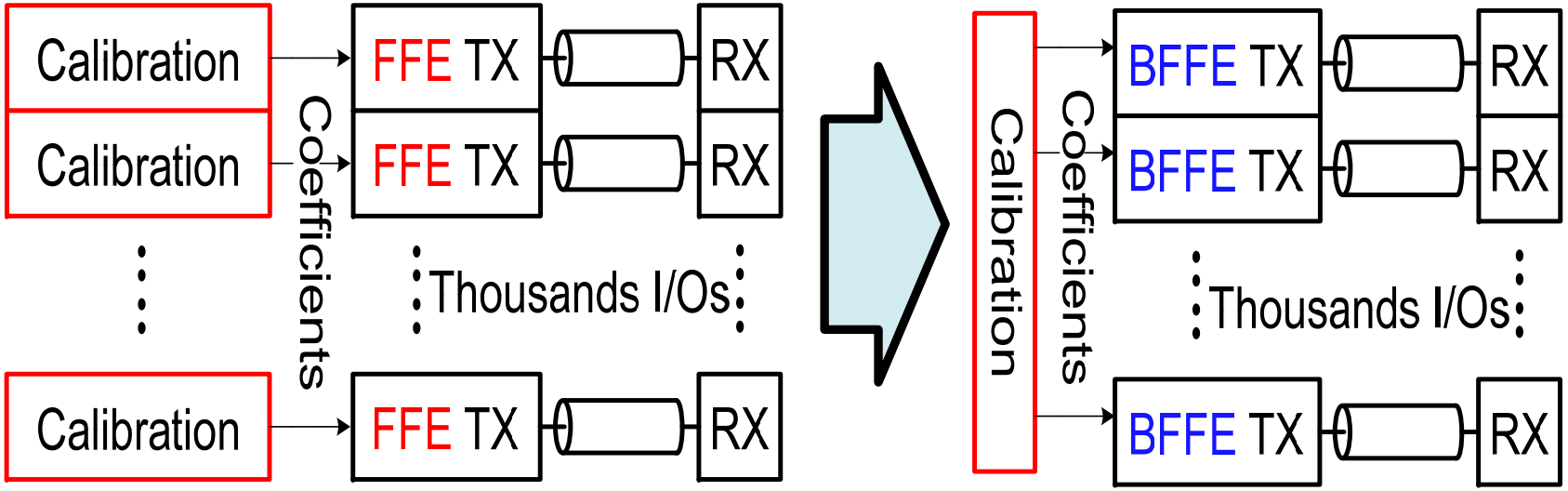
- **Implemented in a DLL-Based reference-less CDR**
  - 0.057 mm^2 in 65nm CMOS
  - Lock range of 6.5-to-9Gb/s with 0.9V supply
  - Power efficiency of 0.63mW/Gb/s

A Coefficient-Error-Robust FFE TX with 230% Eye-Variation Improvement Without Calibration in 65nm CMOS Technology

Seungho Han, Sooeun Lee, Minsoo Choi,
Jae-Yoon Sim, Hong-June Park, and
Byungsub Kim

Department of Electrical Engineering,
POSTECH, Pohang, Korea

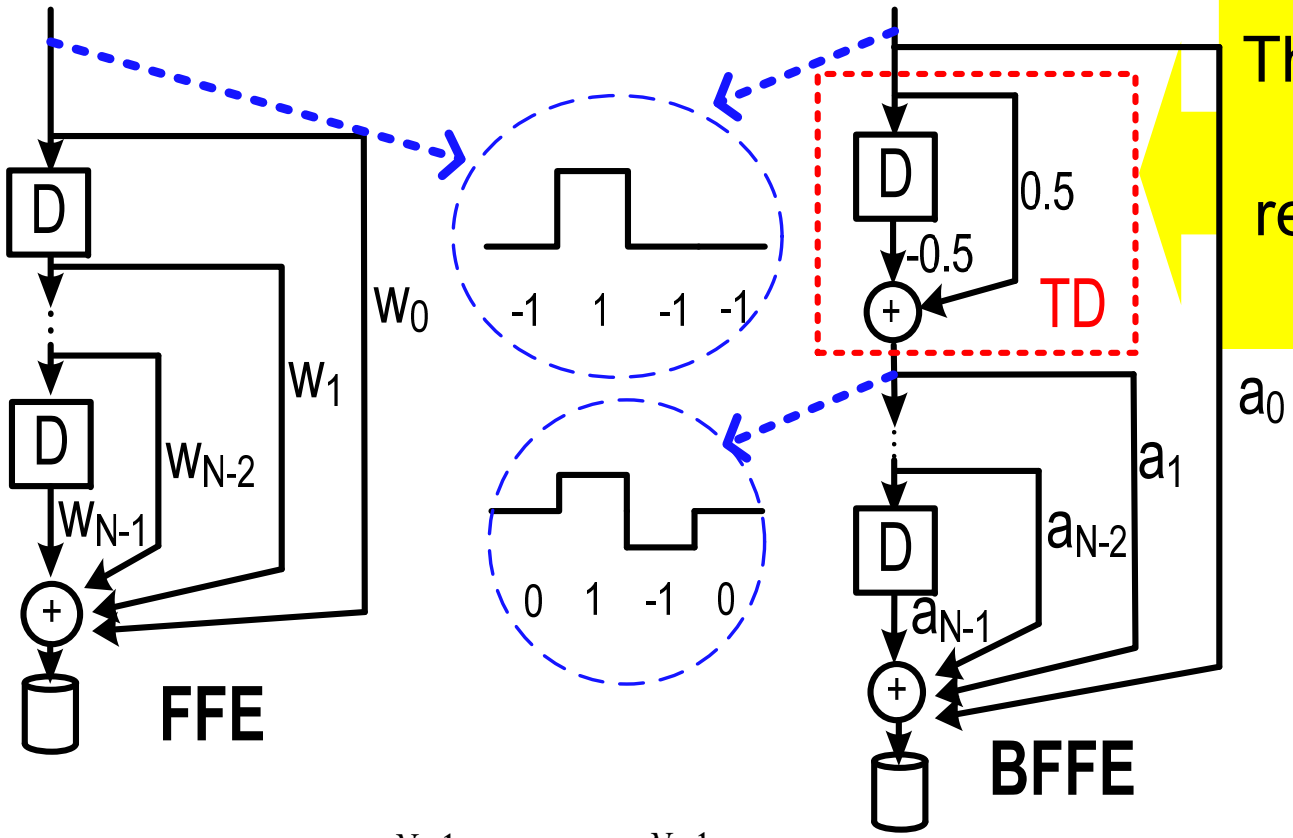
Application: FFE TX in Massively Parallel Links



- Variation & mismatch → Calibration per FFE TX
- Too much HW cost. Eg.)>220% of transceiver cores*
- The proposed BFFE (FFE TXs robust to mismatch) can amortize calibration overhead.

* S. Lee et al., "A 95fJ/b Current-Mode Transceiver for 10mm On-Chip Interconnect," *ISSCC, Feb 2013, pp. 262-263.*

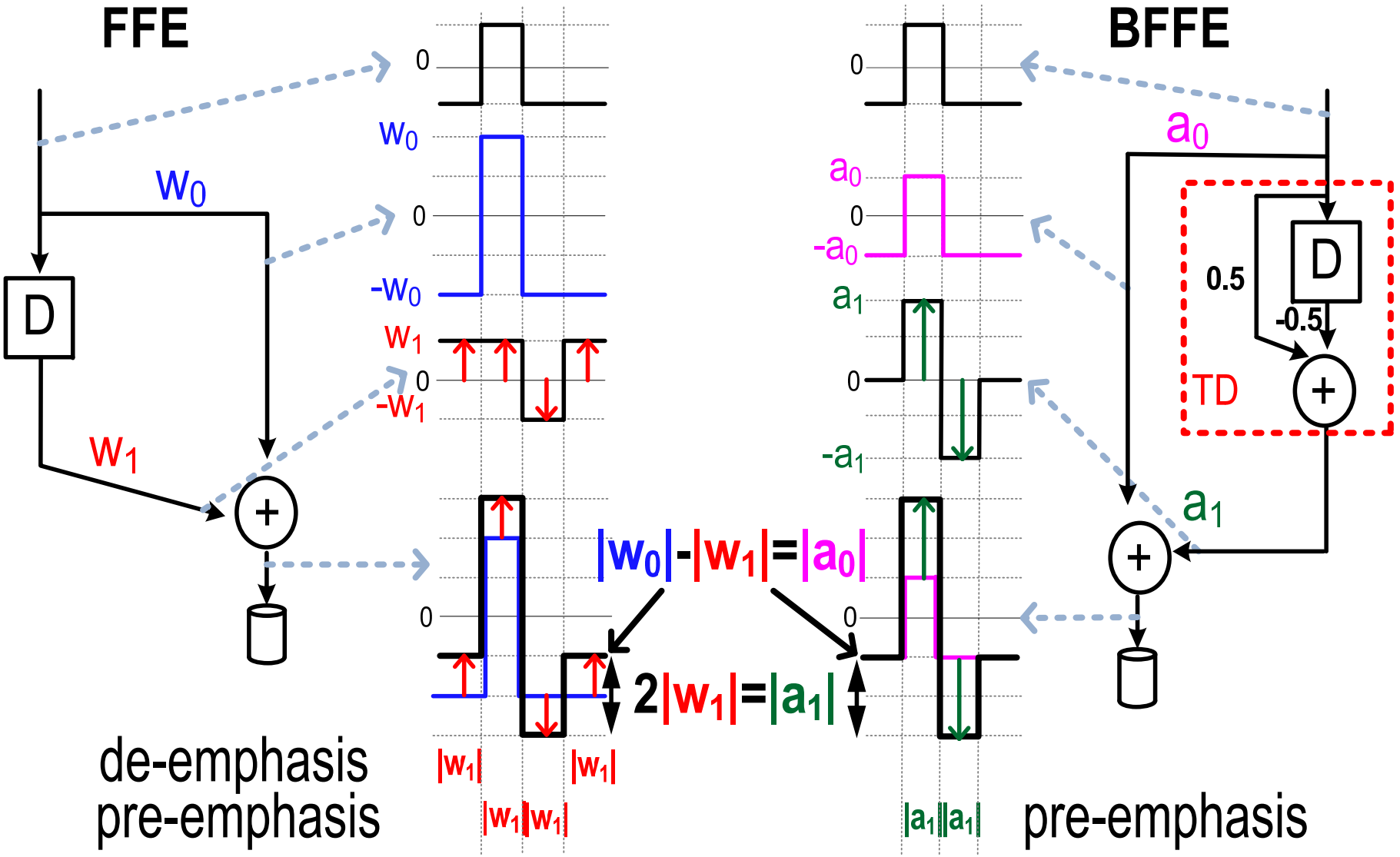
Conventional FFE vs. Coefficient-Error-Robust FFE(BFFE)



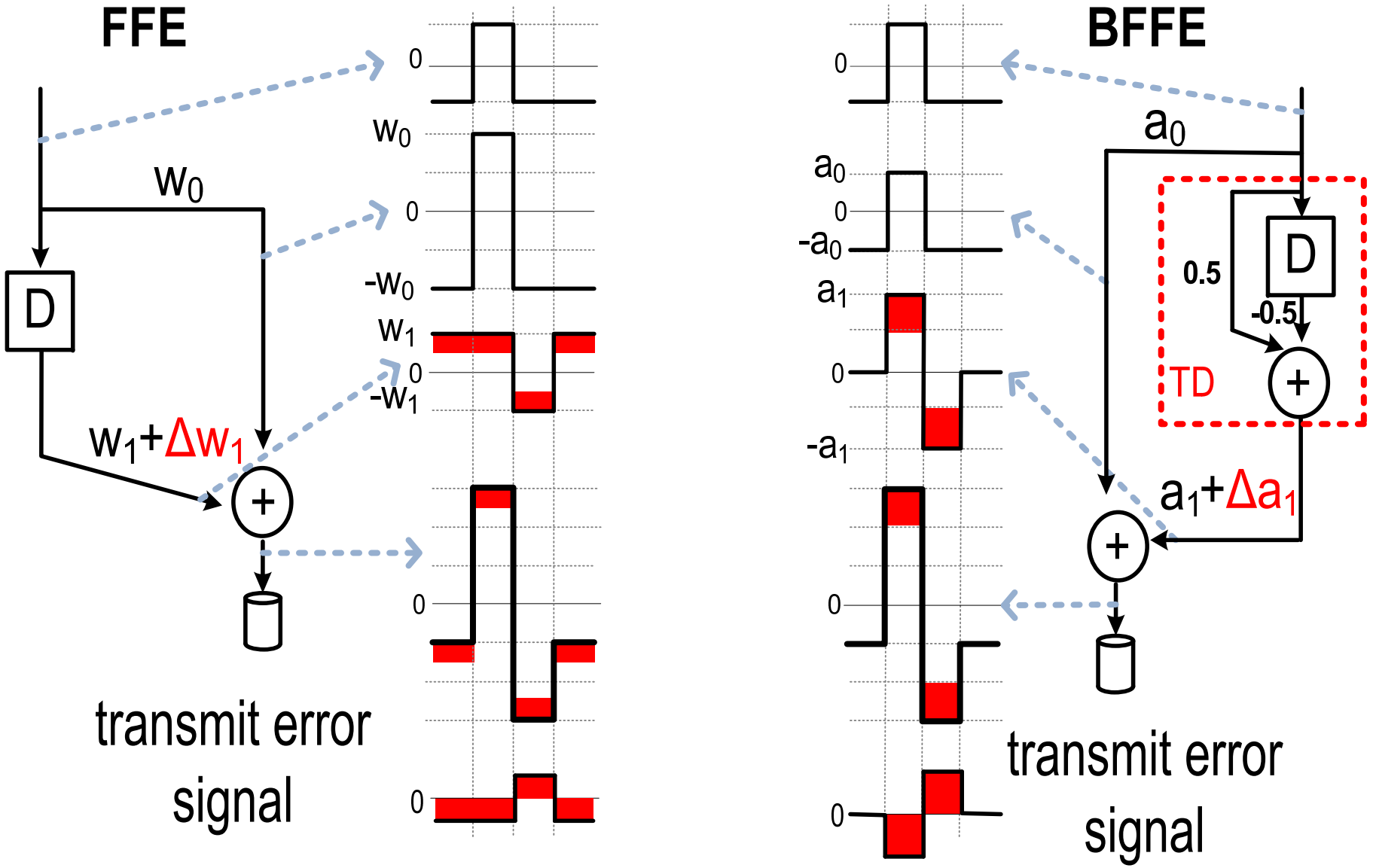
The first delay unit is replaced with a TD filter.

$$a_{k\neq 0} = -2\sum_{i=k}^{N-1} w_i \, a_0 = \sum_{i=0}^{N-1} w_i \rightarrow \text{identical output}$$

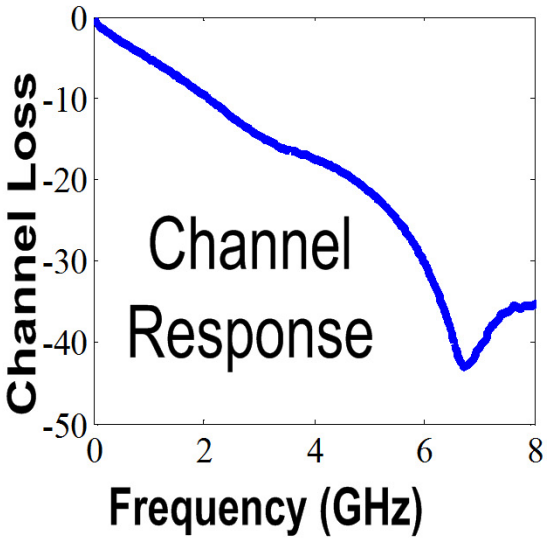
Example: 2-Tap FFE vs. BFFE

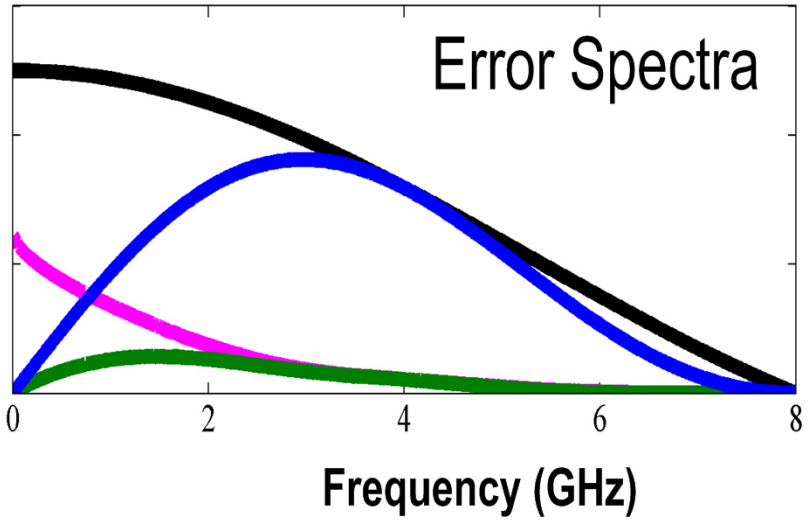


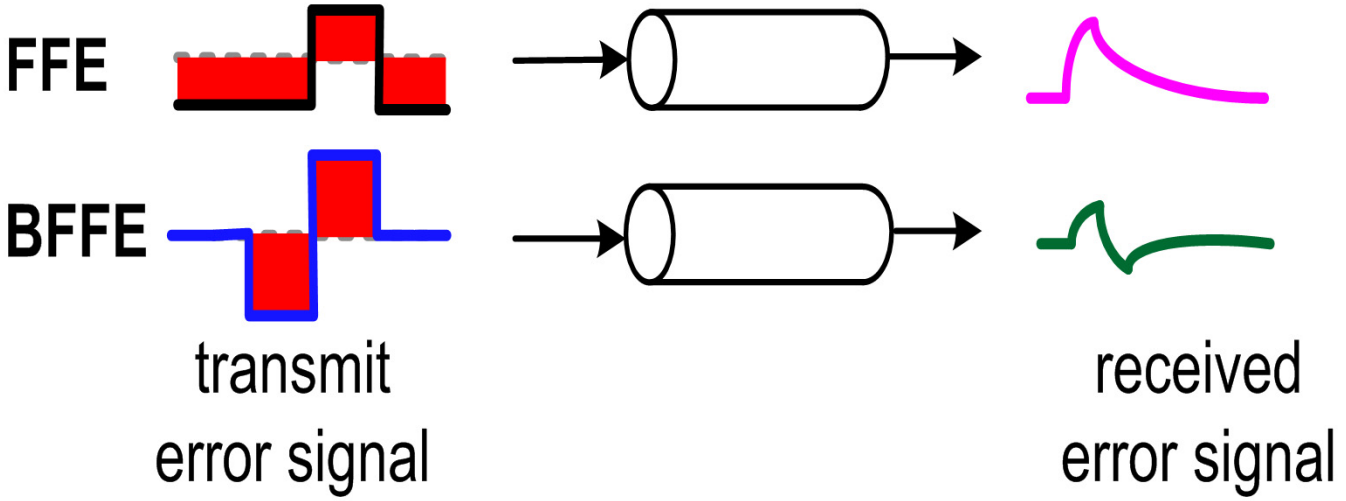
TX Error Signal by A Coefficient Error



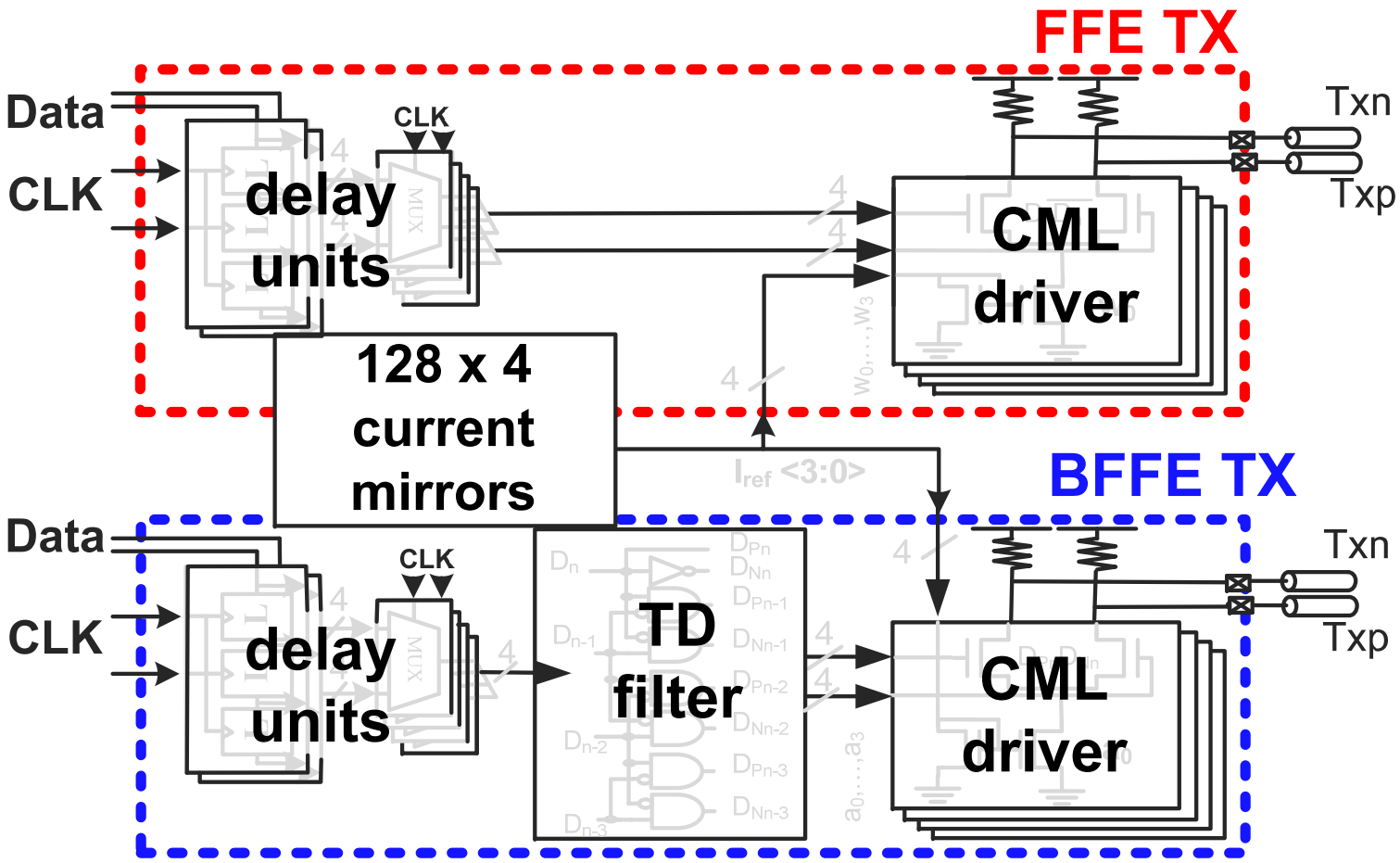
Error Suppression Mechanism





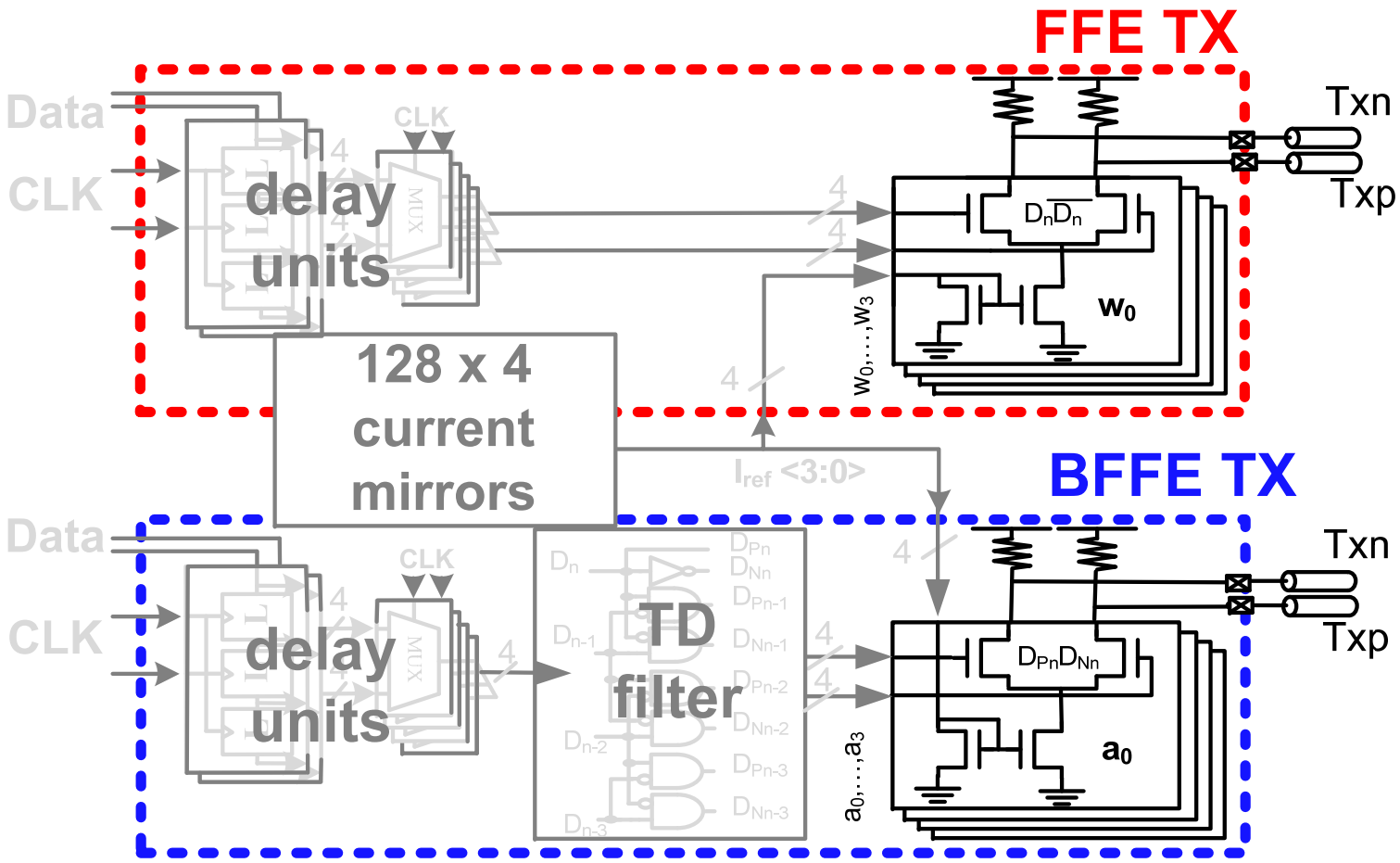


Chip Implementation



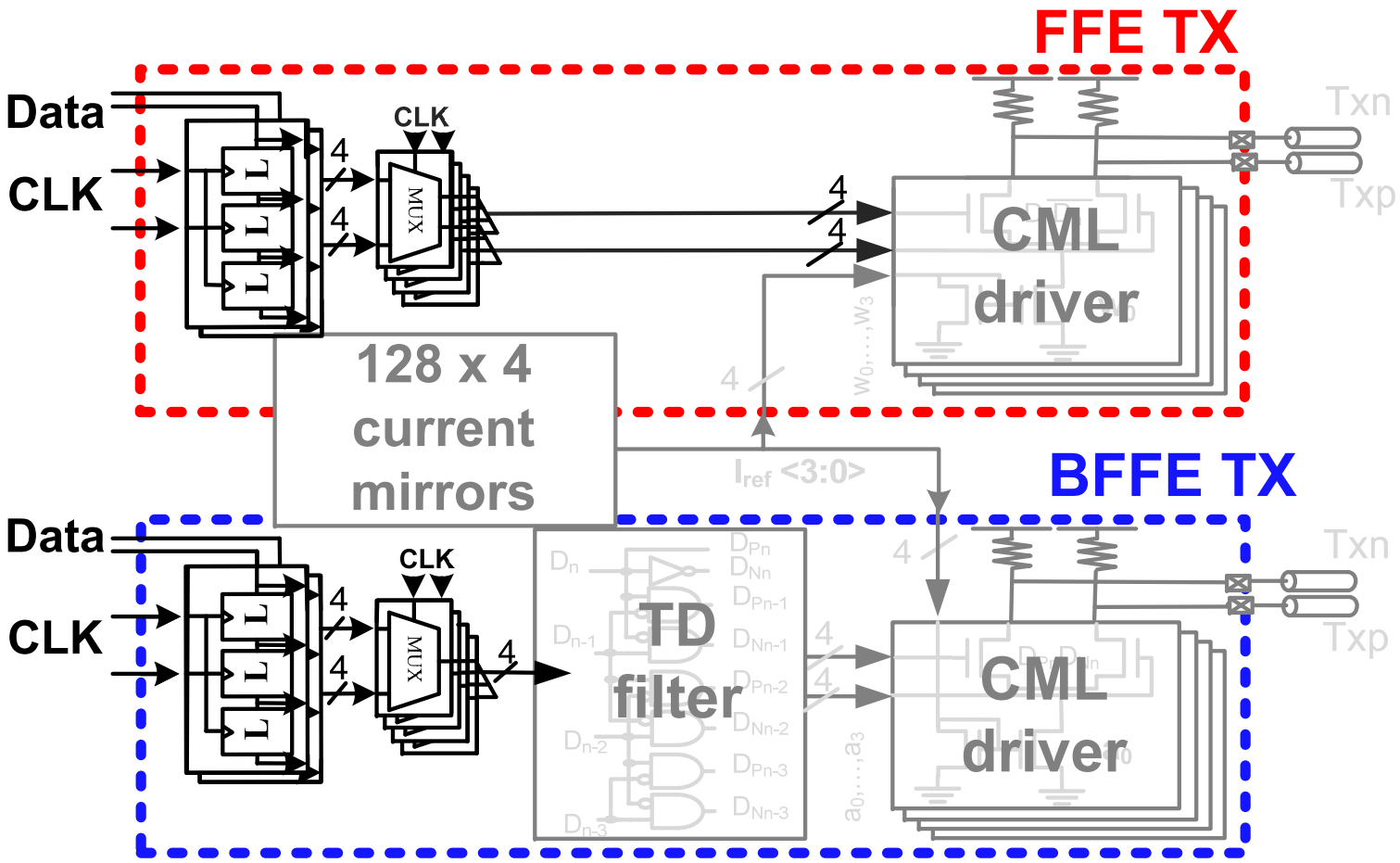
- 4-tap FFE and B-FFE TXs

Driver



- 50-Ω CML-type drivers for both TXs

Delay Units



- Latch-based half rate architecture

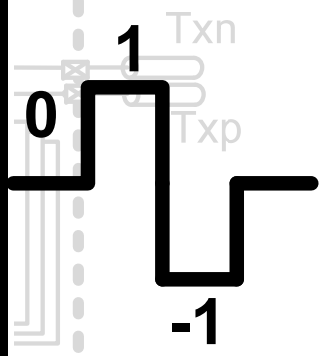
TD Filter

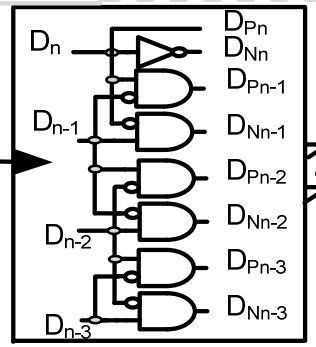
D_nD_{n-i}	$D_{Pn-i}D_{Nn-i}$	level
10	10	1
00	00	0
11	00	0
01	01	-1

outputs

current bit

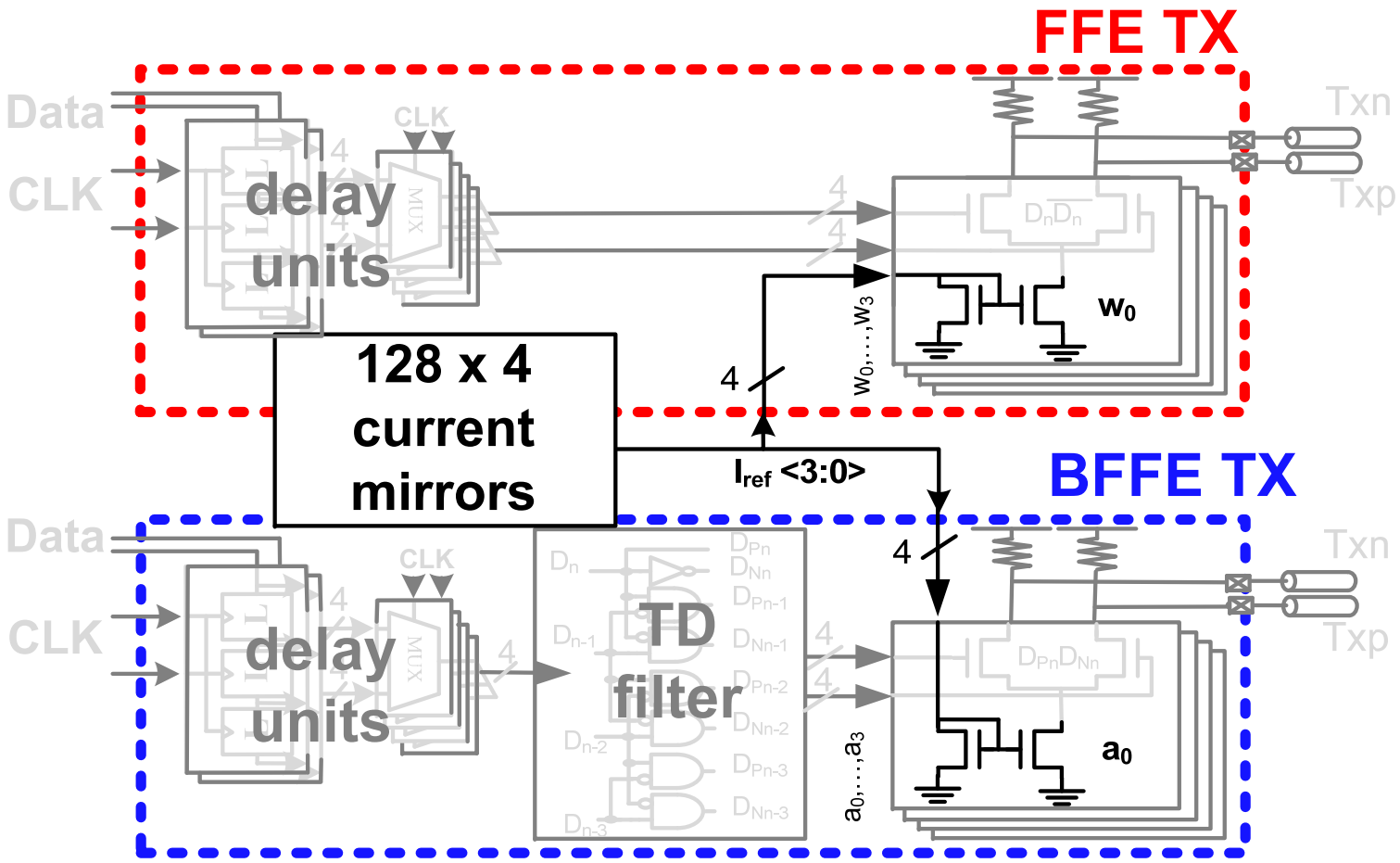
previous bit





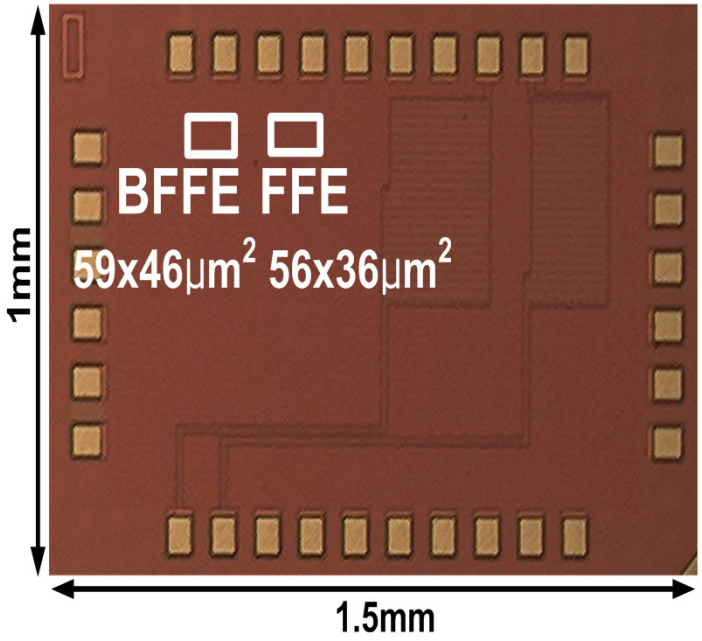
- Standard CMOS digital gates are used for TD
- 2-bit encoding for 3 levels of TD output

Current Sources



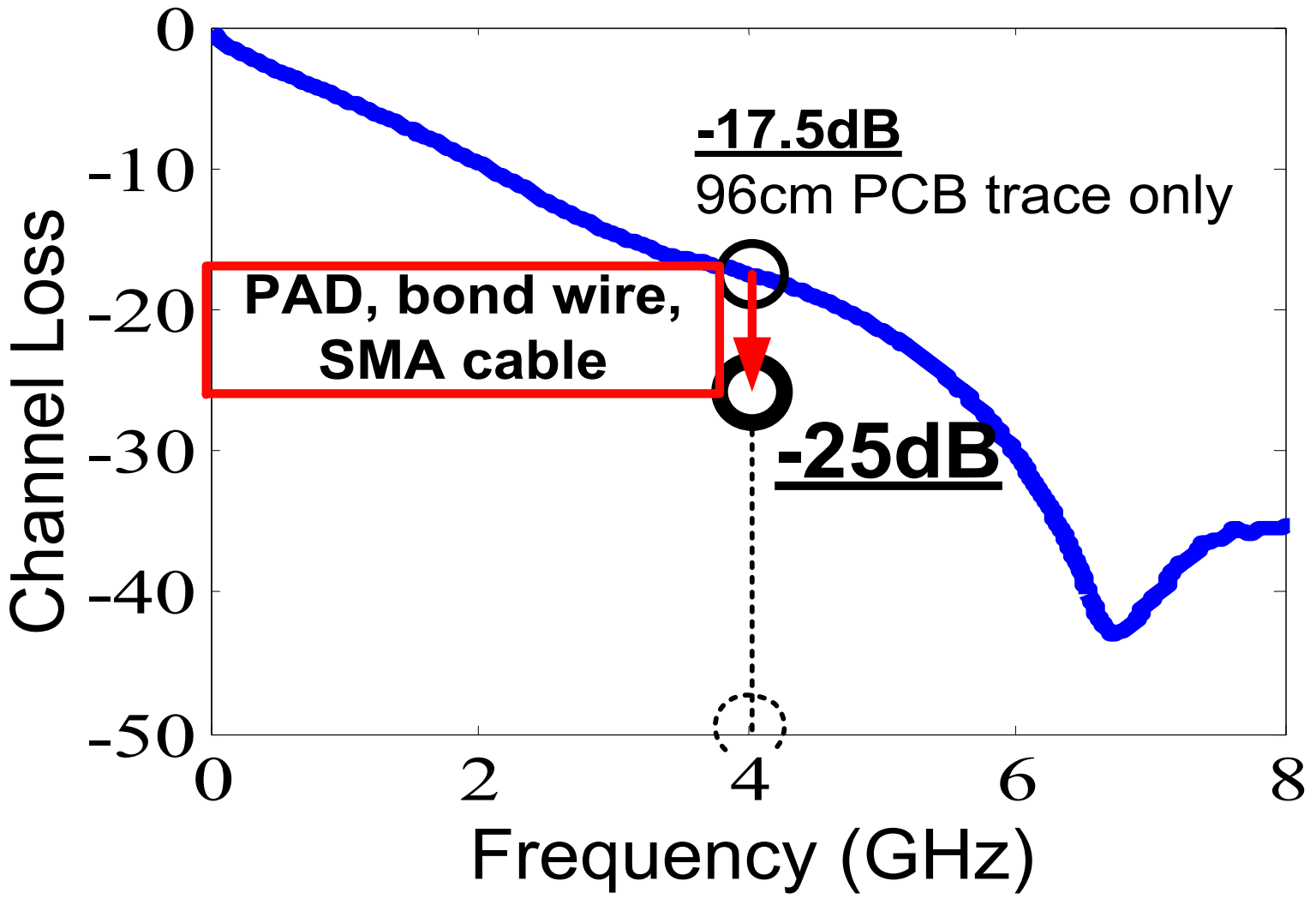
- 128 sets of current mirrors for statistical coefficient mismatch measurement.

Die Micrograph

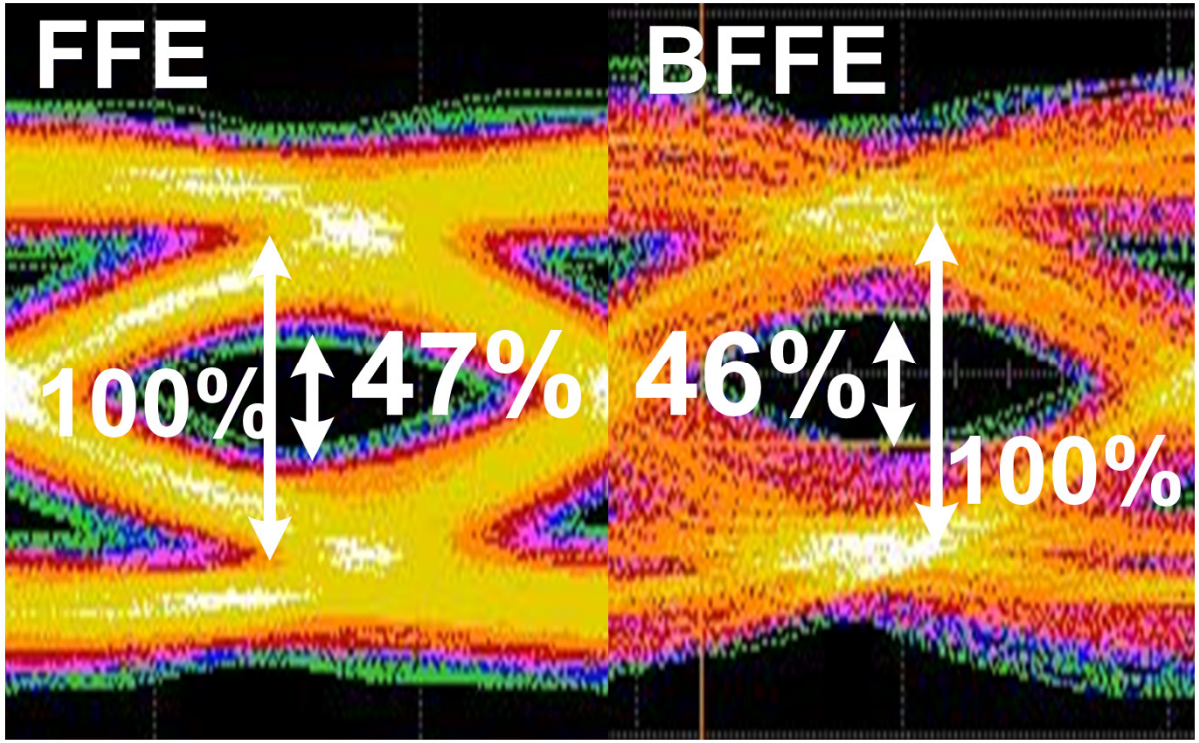


- 65nm bulk CMOS technology

Channel Transfer Function



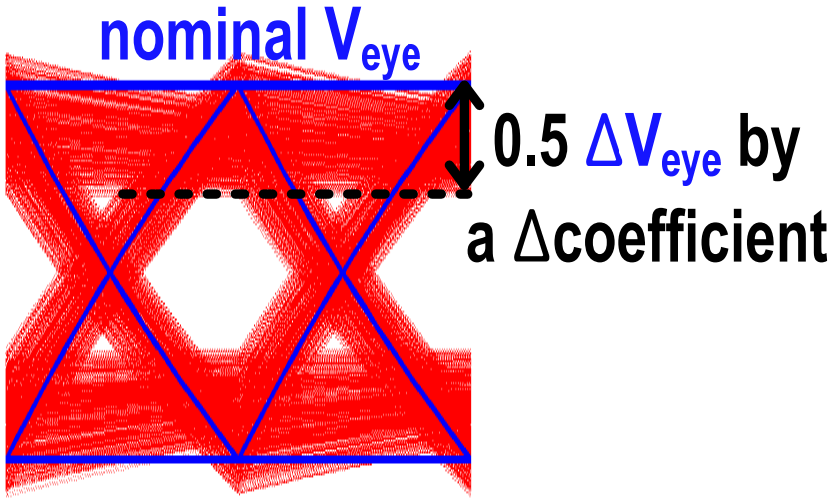
Nominal Eye Measurement



- 8Gb/s
- PRBS-31
- 96cm PCB trace + PADs + bond wire

Eye Sensitivity Measurement

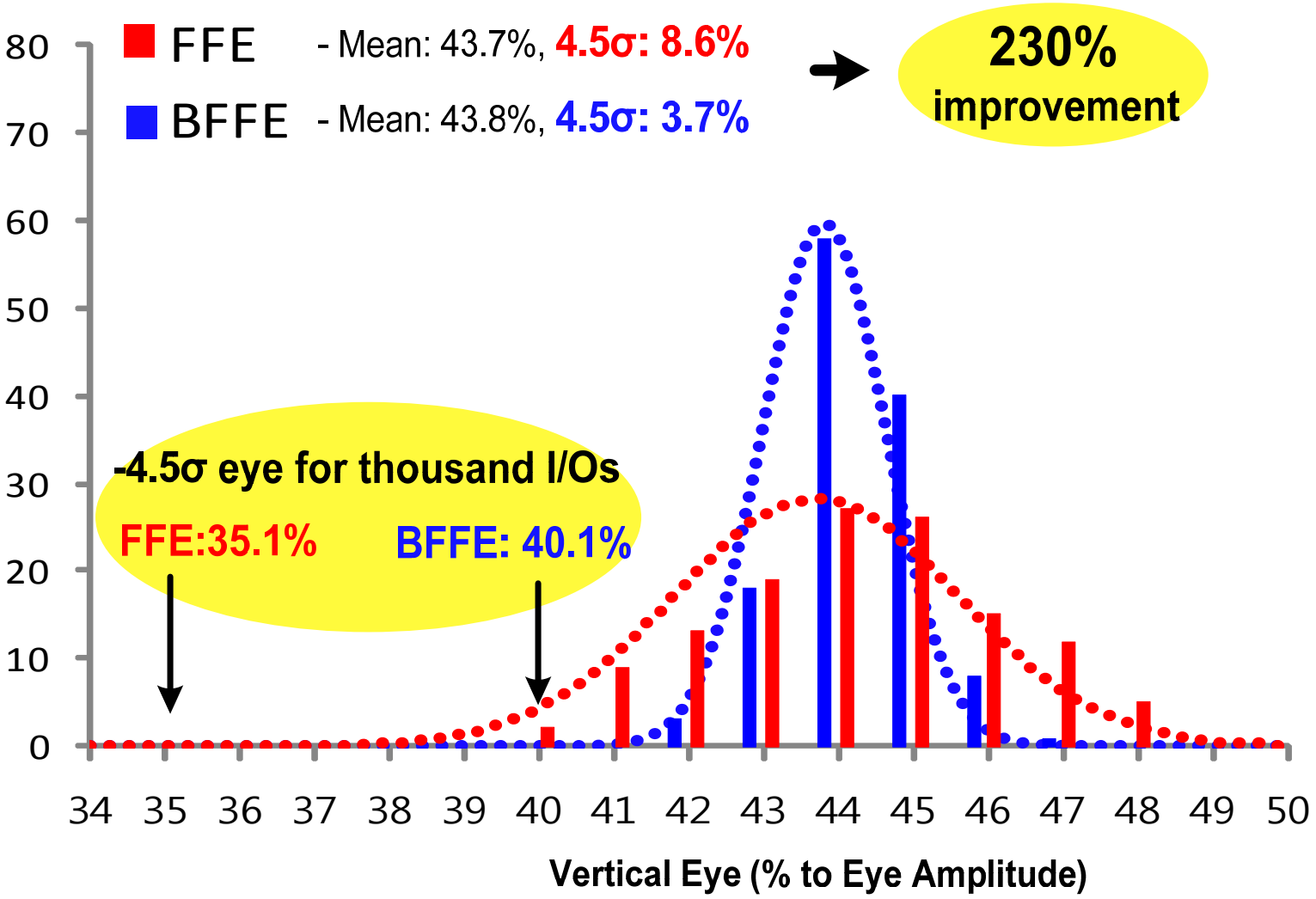
$$\text{eye sensitivity} = \frac{\left|\frac{\Delta V_{eye}}{V_{eye}}\right|}{\left|\frac{\Delta \text{coefficient}}{\text{coefficient}}\right|}$$



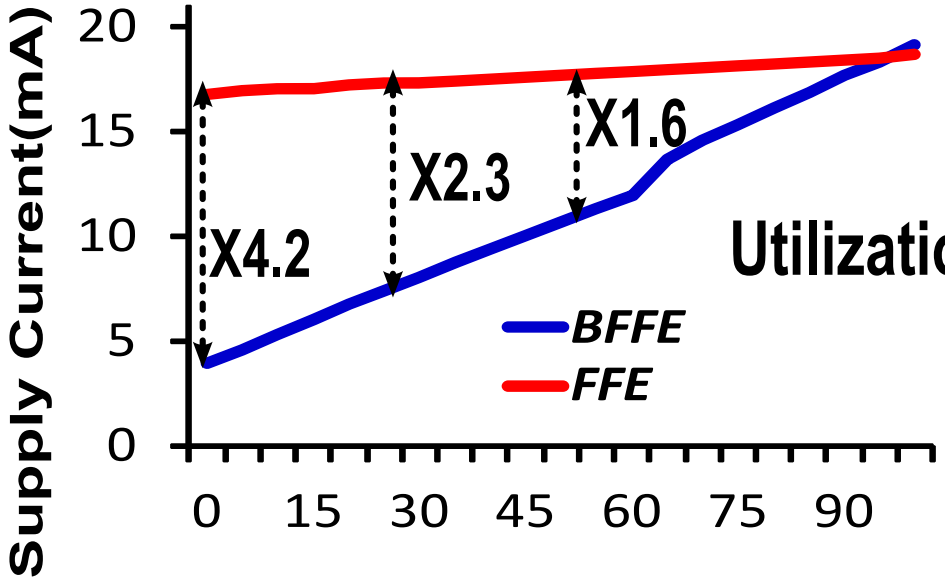
FFE sensitivity = 1.35, BFFE sensitivity = 0.56

→ BFFE's eye sensitivity is 2.4 times improved than FFE.

Measured Eye Variation Histogram

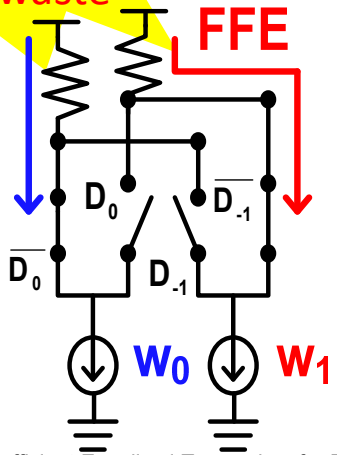


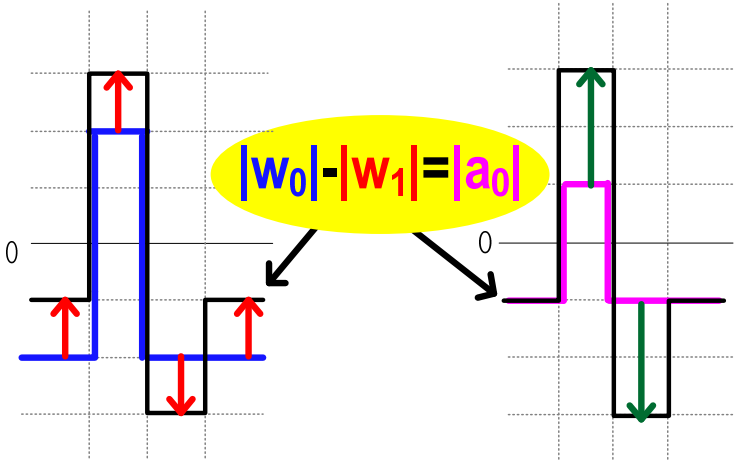
Supply Current vs. Utilization

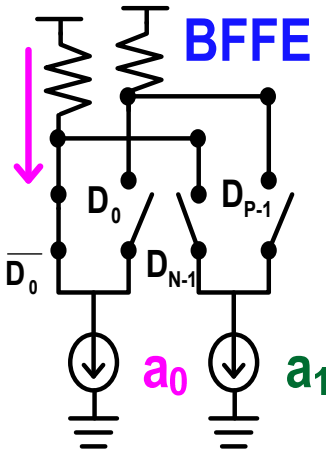


$$\text{Utilization} = \frac{T_{USAGE}}{T_{USAGE} + T_{IDLE}}$$

De-emphasis: current waste





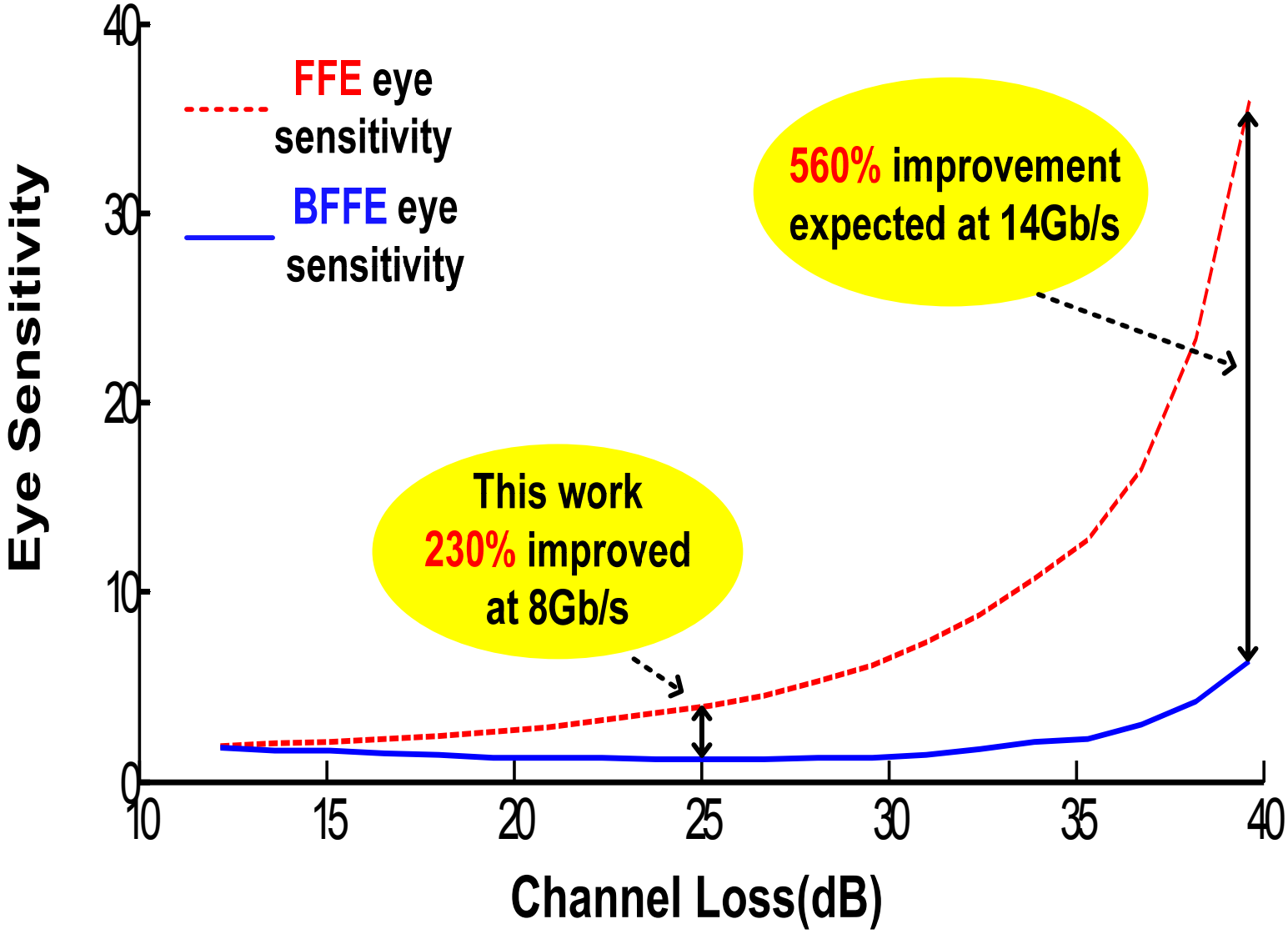


B. Kim et al., "An Energy-efficient Equalized Transceiver for RC-dominant Channels," *IEEE JSSC, vol. 45, no. 6, pp. 1186-1197, June 2010.*

Performance Summary

		FFE	BFFE
technology		65nm	65nm
supply voltage		1.3V	1.3V
data rate		8Gb/s	8Gb/s
96cm PCB channel loss		25dB	25dB
vertical eye (average)		43.7%	43.8%
supply current	100% util.	17.3mA	16.7mA
	25% util.	17.3mA x2.3	7.4mA
worst eye sensitivity		1.35 →	0.56
4.5-σ eye deviations		8.6%	3.7%
area		2128um^2	2714um^2

Eye Sensitivity Projection



Conclusion

- A coefficient-error-robust FFE(BFFE) TX is proposed.
  - ➢BFFE and FFE behave identically at nominal.
  - ➢A cheap digital TD filter of BFFE utilizes channel loss to suppress signal perturbation by coefficient errors.
- BFFE improves eye variation by 230% at 8Gb/s over 25dB channel.
- BFFE improves power consumption by 230% with 25% utilization.
- Larger eye variation improvement (560%) is expected at higher loss (40dB).

A Pulse-Position-Modulation Phase-Noise-Reduction Technique for a 2-to-16GHz Injection-Locked Ring Oscillator in 20nm CMOS

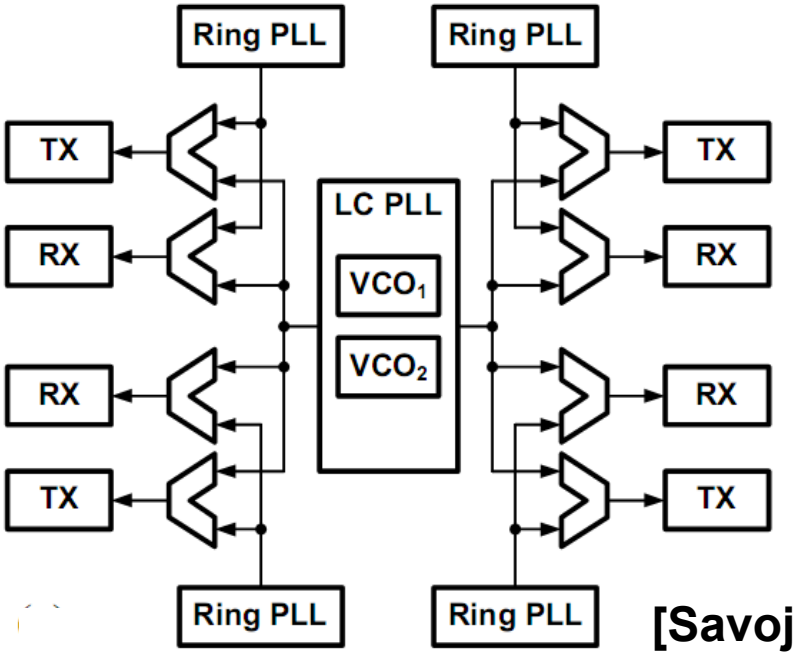
Jun-Chau Chien[1], Parag Upadhyaya[2], Howard Jung[2], Stanley Chen[2], Wayne Fang[2], Ali M. Niknejad[1], Jafar Savoj[2], Ken Chang[2]

[1]University of California, Berkeley, CA

[2]Xilinx, San Jose, CA

Motivation

FPGA Quad Transceiver Architecture



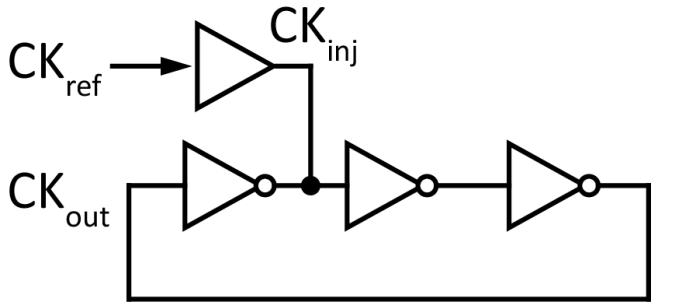
	LC-PLL	Ring-PLL
Area	Large	Small
Range	Narrow	Wide
Jitter	Low	High

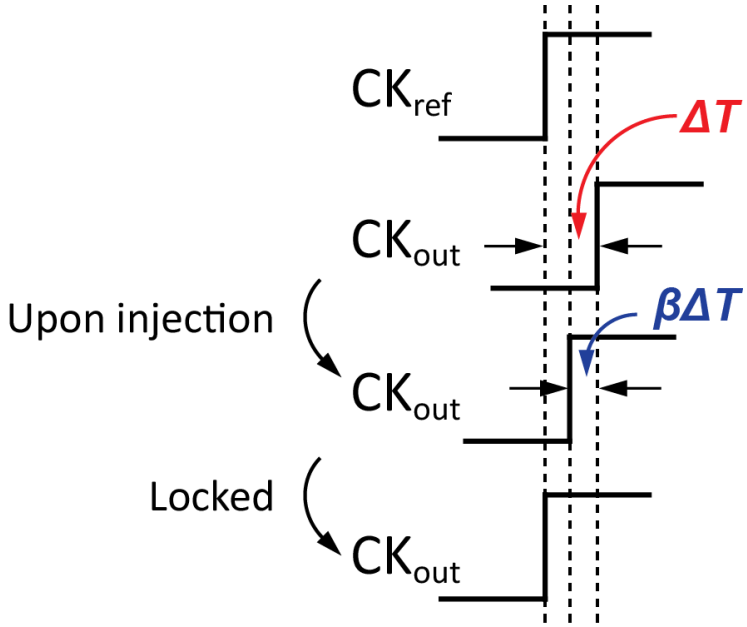
[Savoj, CICC'12]

- FPGA requires large number of reconfigurable transceivers

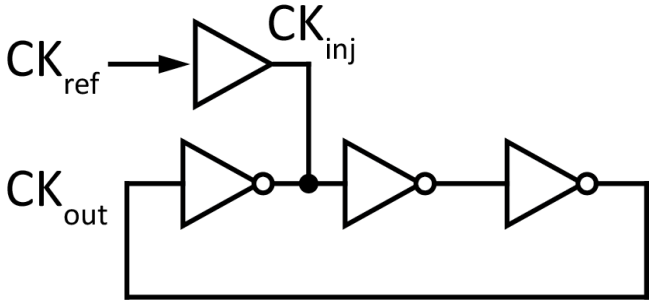
Target: Ring-based clock gen. with LC-PLL jitter

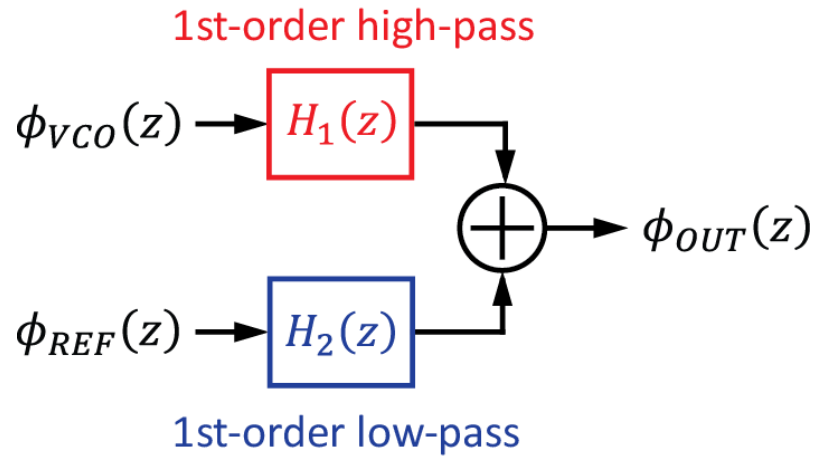
Injection-Locking

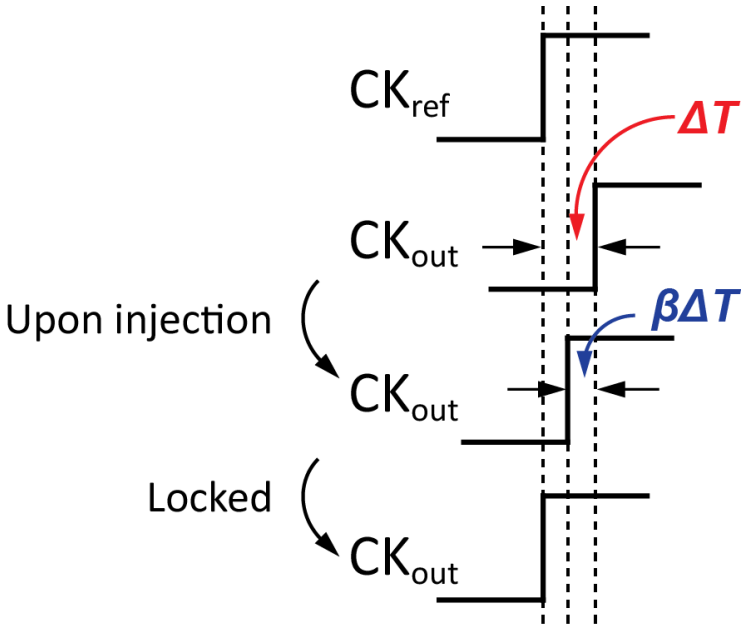


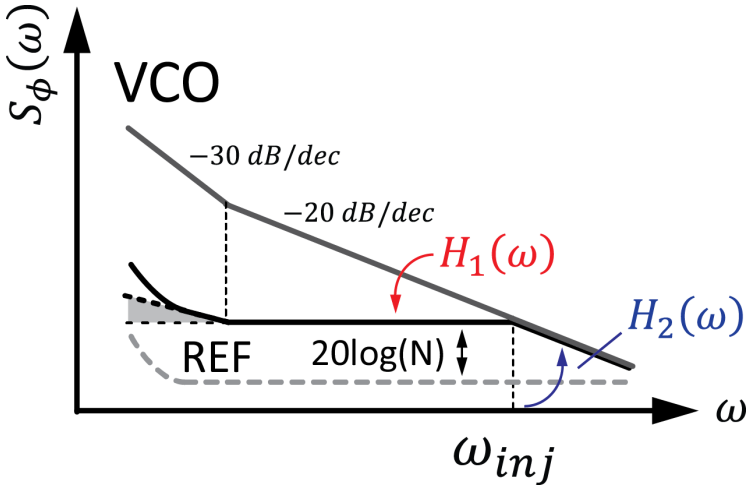


Injection-Locking





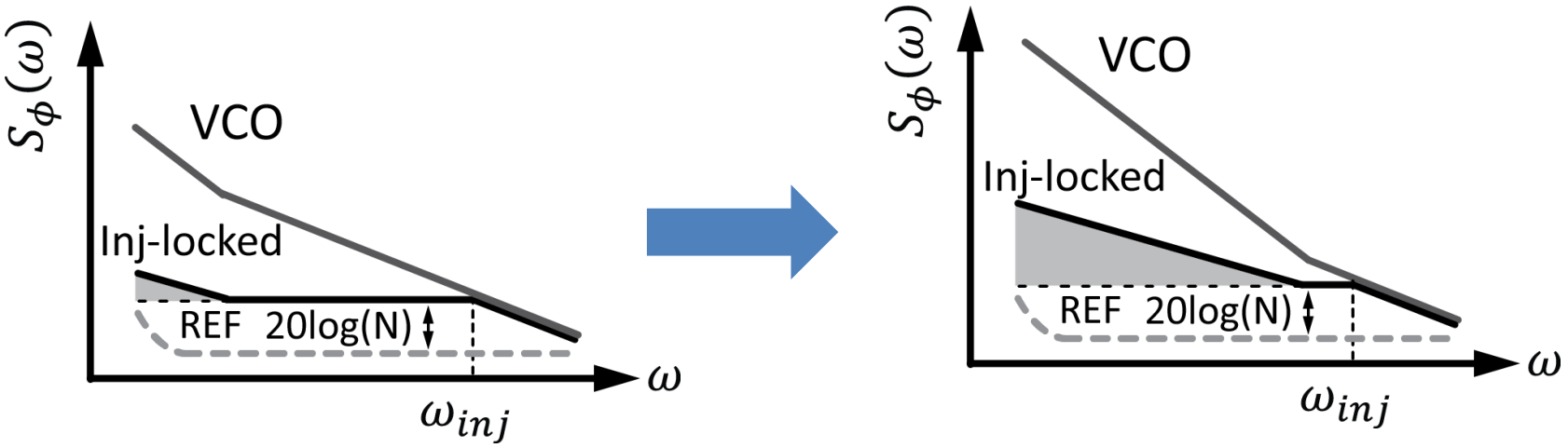




- **Better VCO noise rejection ($\beta F_{ref}/4$) vs. PLL ($F_{ref}/10$)**

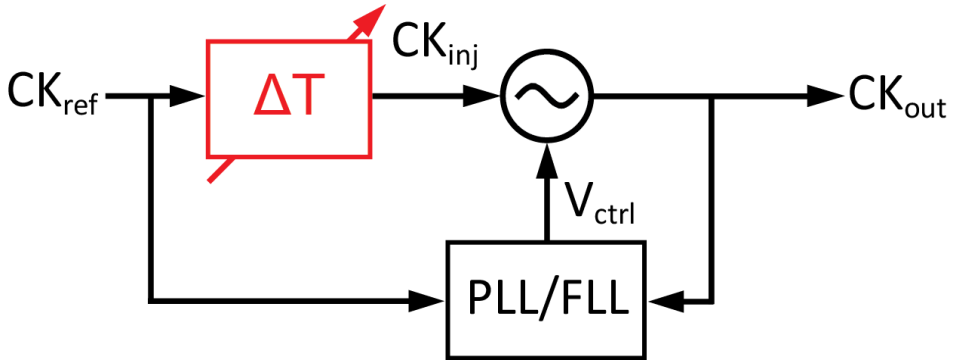
VCO Flicker Noise

- High $1/f^3$ corner frequency (tens of MHz) in 20nm
- Up-sizing inverter width is not effective

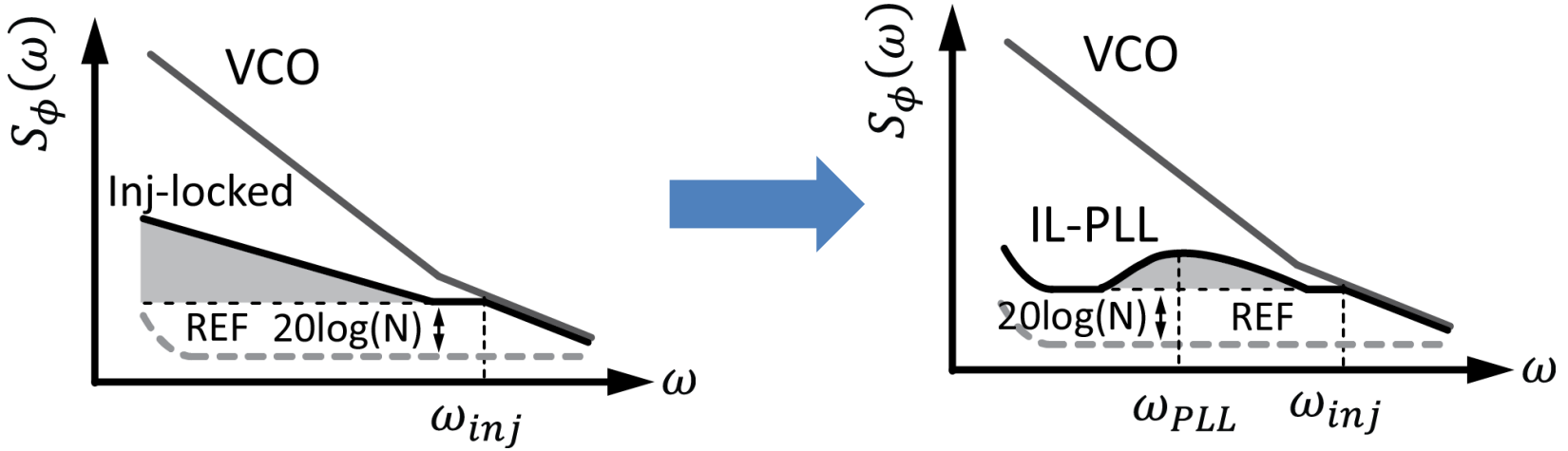


Need 2nd-order noise shaping for VCO $1/f^3$ noise

Injection-Locked PLL

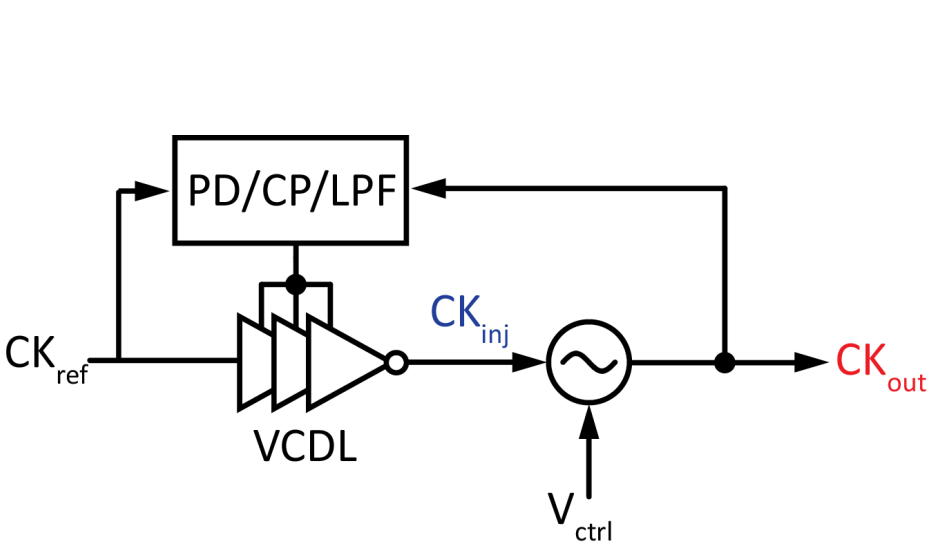


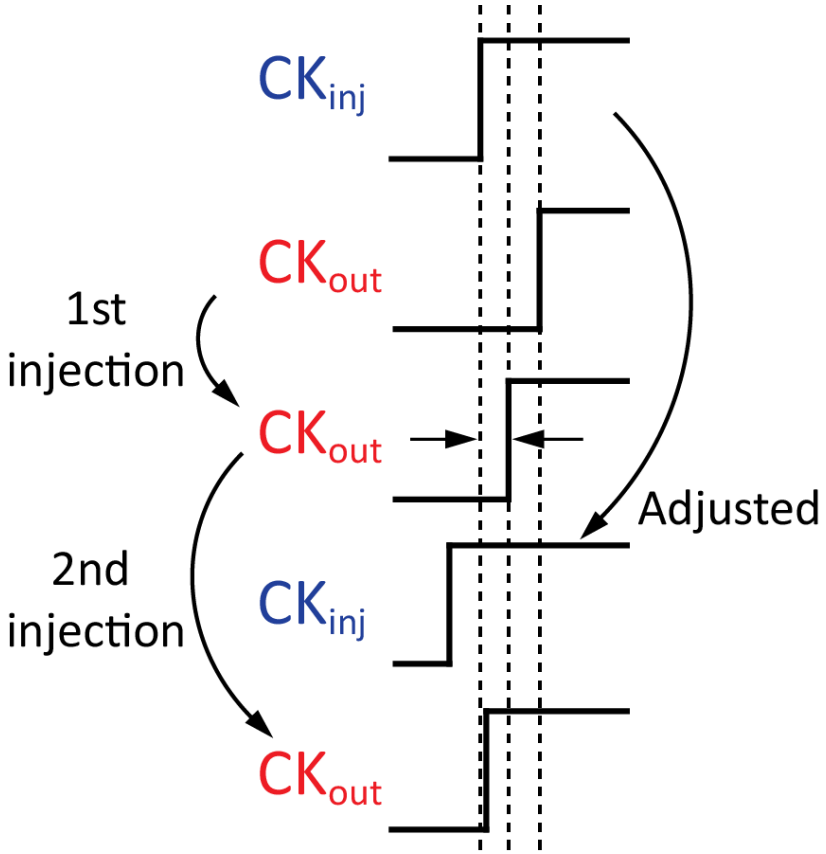
[ISSCC: Lee, '09, Huang, '12, Elshazly, '12]



- **Insufficient rejection due to limited PLL bandwidth**

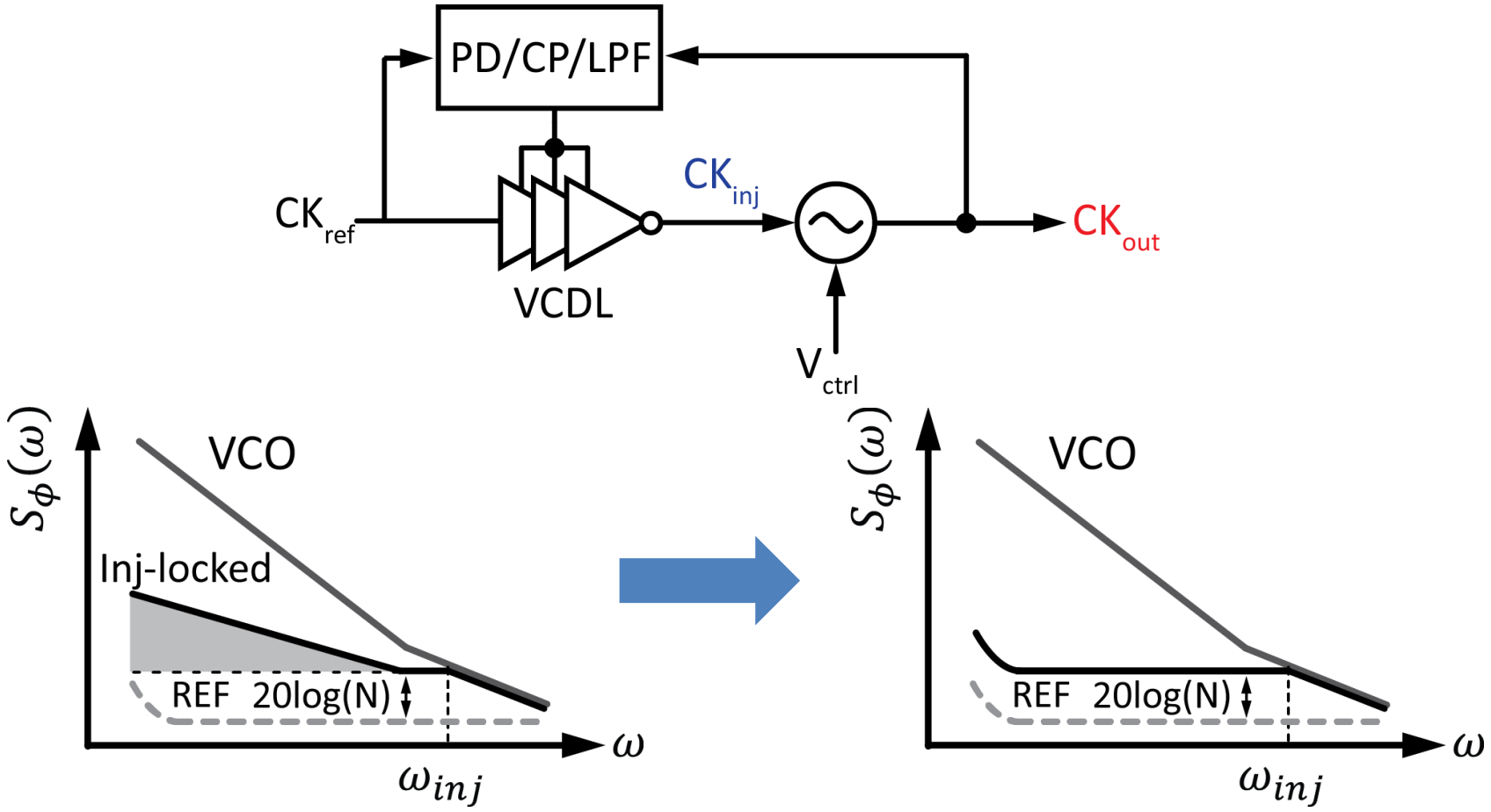
Pulse-Position-Modulation





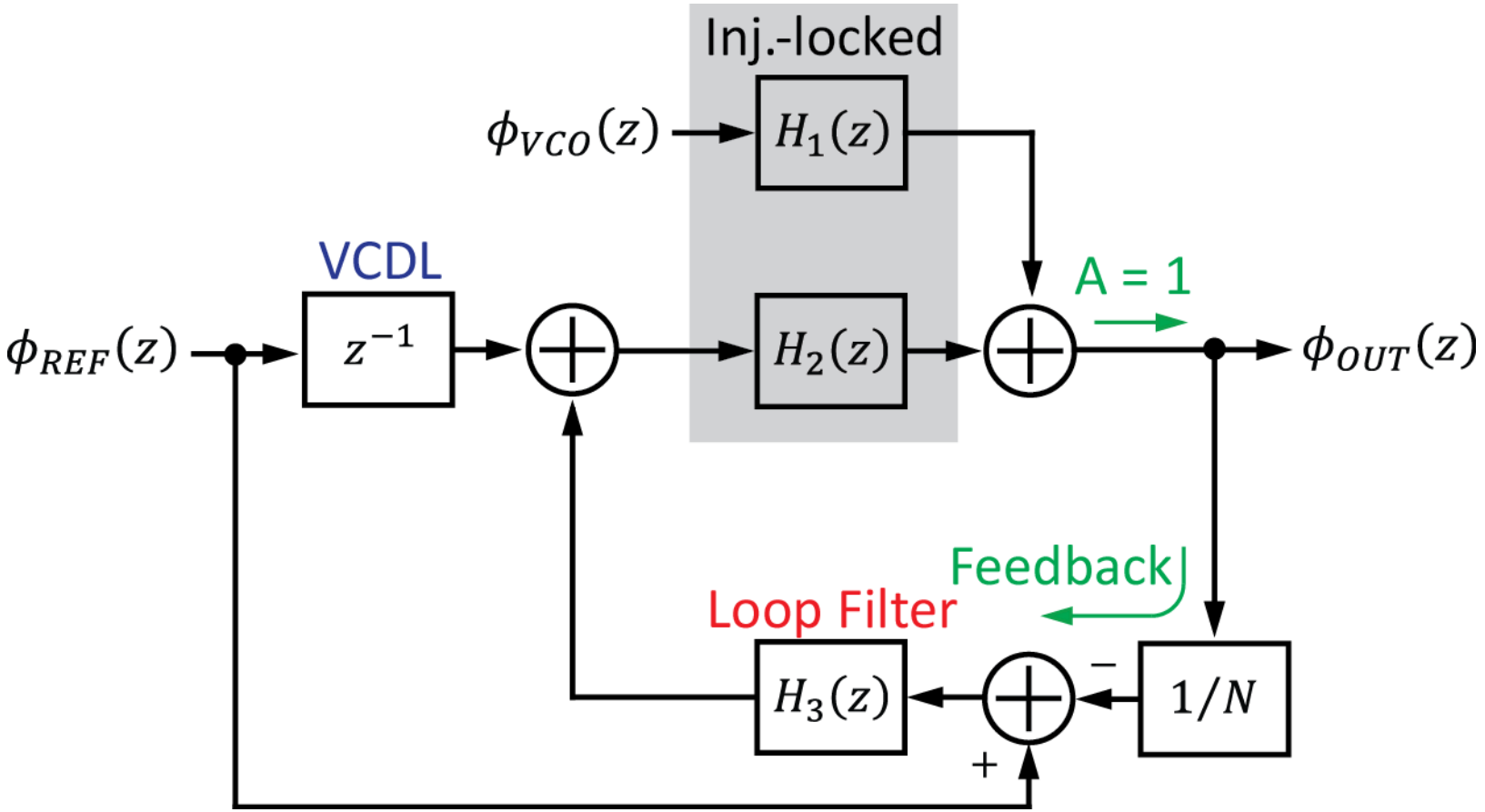
- **Phase error is reduced at a faster rate**

Pulse-Position-Modulation



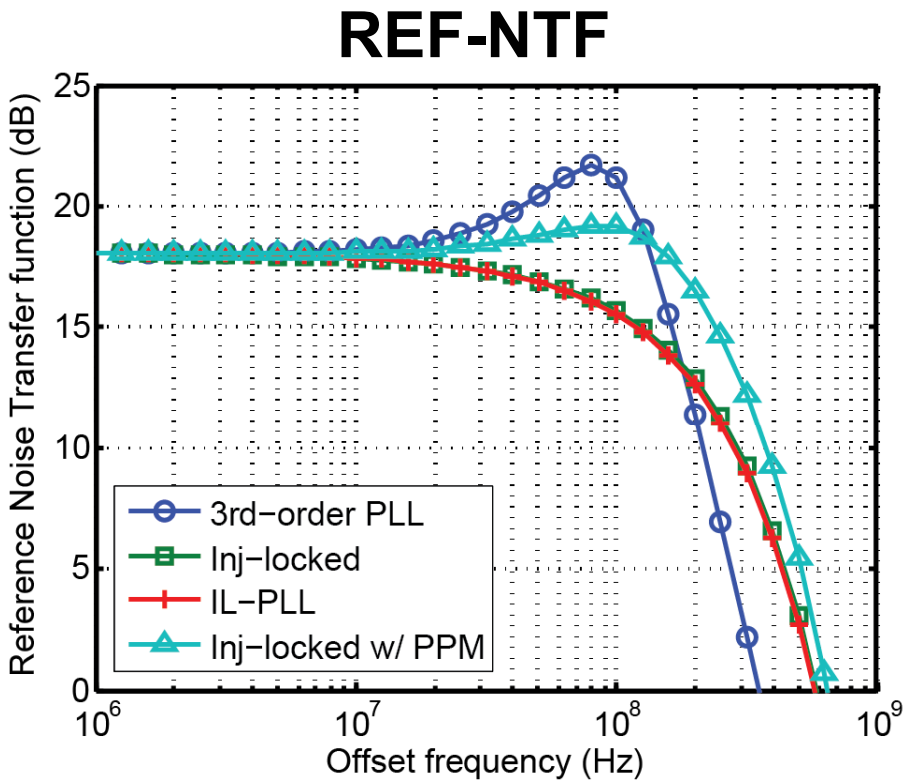
- **Injection phase is modulated to produce a 2nd-order shaping effect**

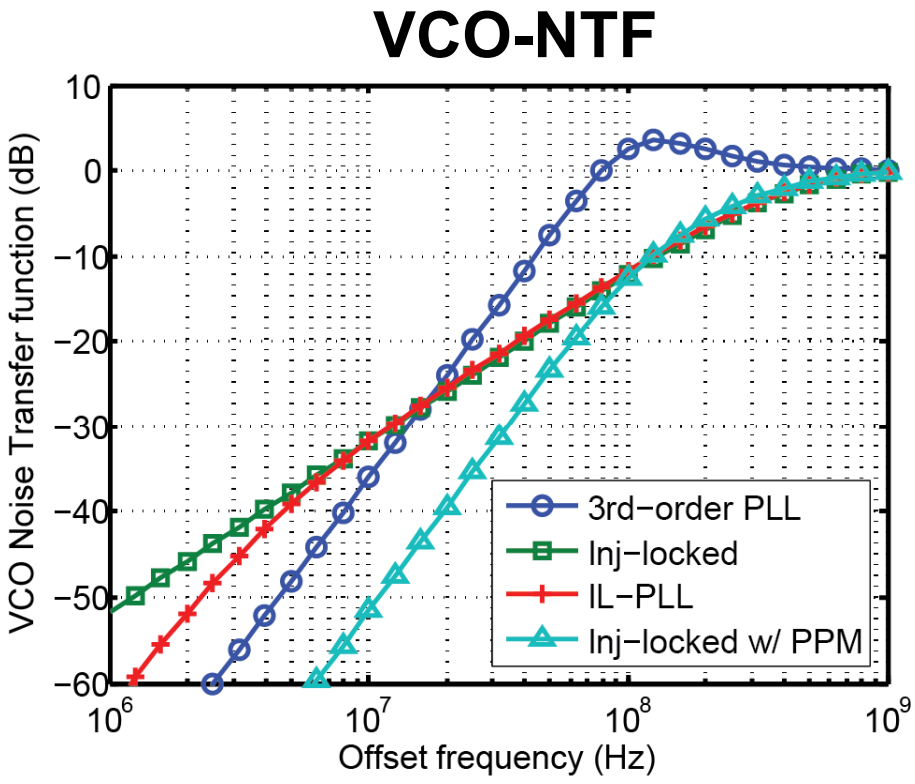
Phase Noise Transfer Function



- **VCO NTF is considered a cascade of two 1st-order high-pass filters**

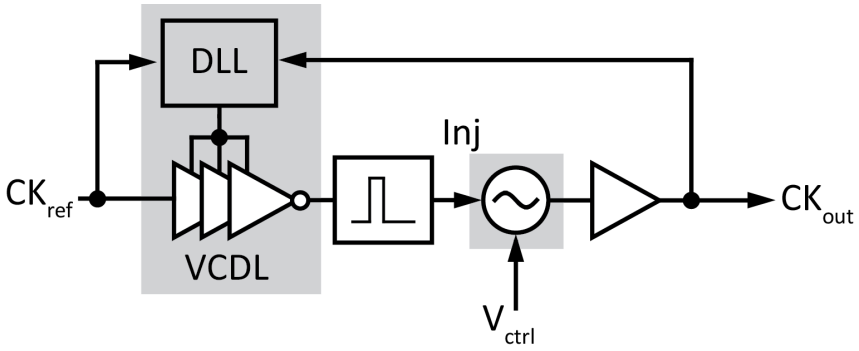
Transfer Curve Comparison



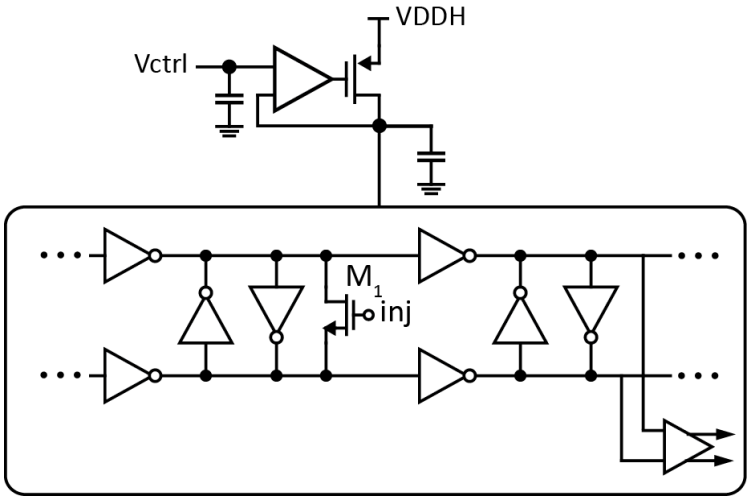


- **Achieve wideband 40 dB/dec filtering when the loop gain is backed off from the stability limit by 4.8x**

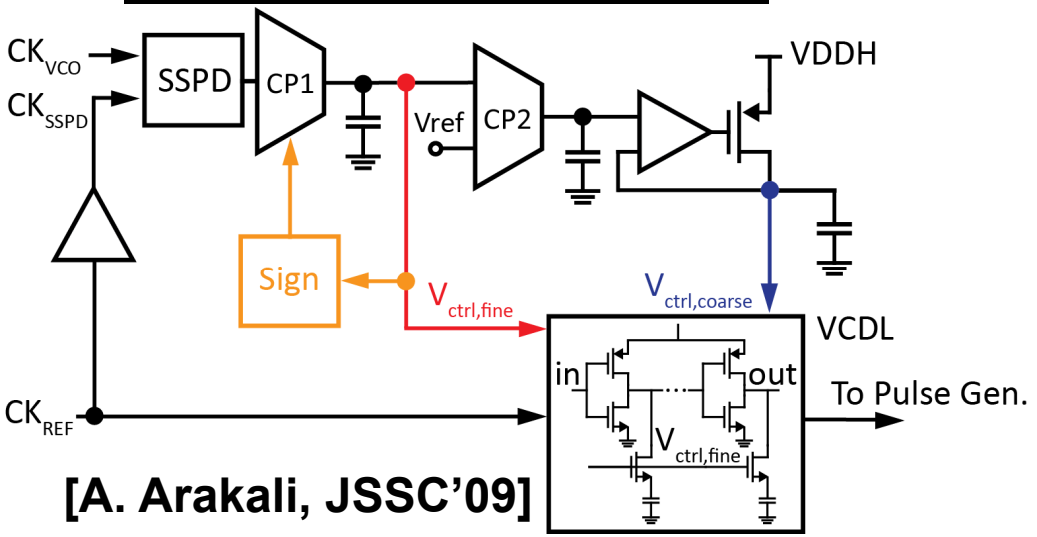
Prototype Implementation



4-stage I/Q ring oscillator



Split-tuned DLL architecture

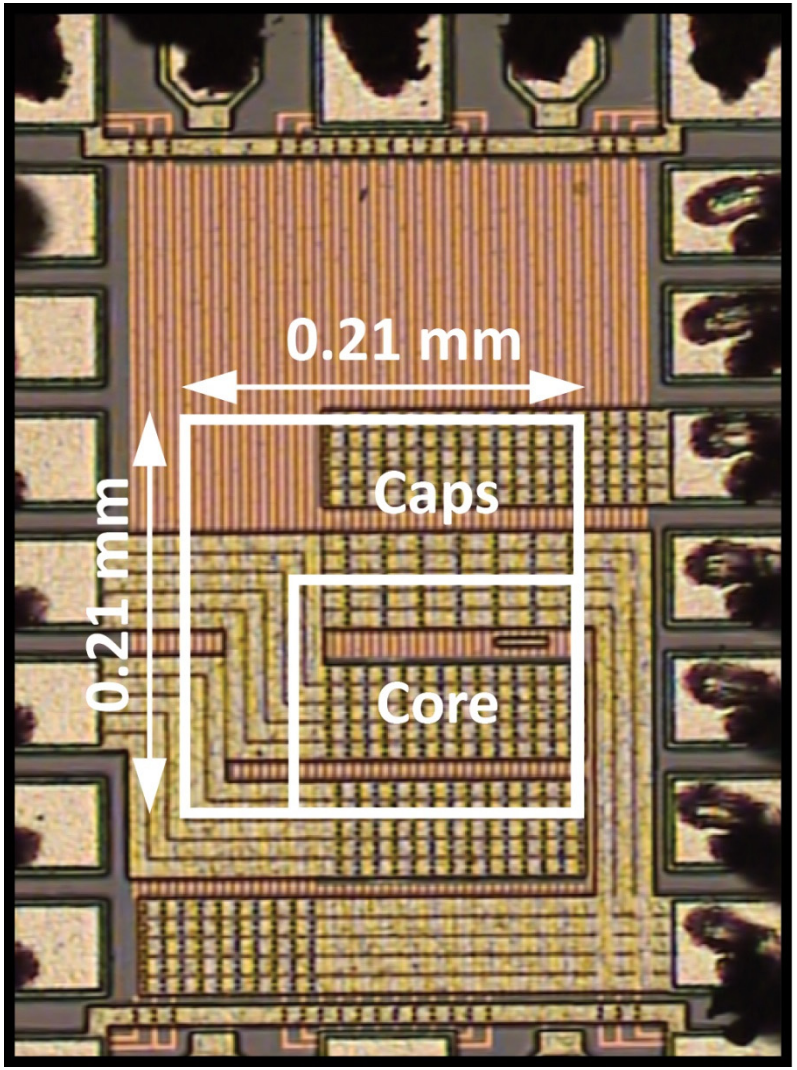


[A. Arakali, JSSC'09]

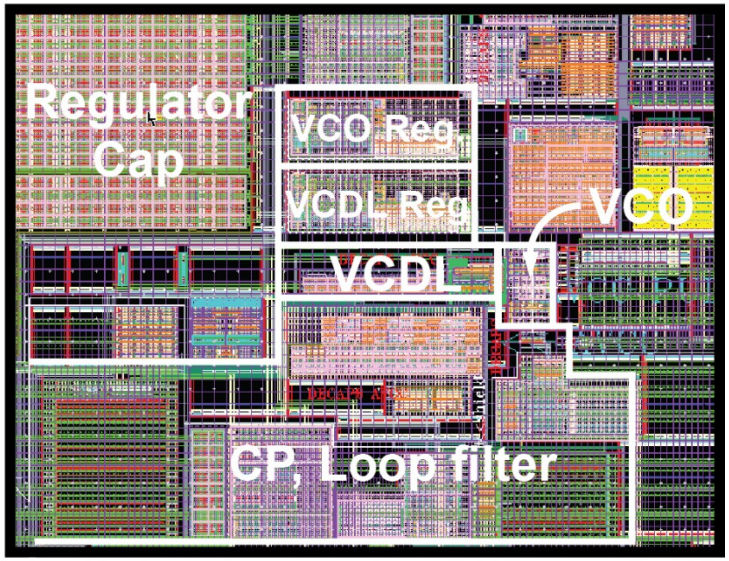
Inj. Strength (β): 0.5 – 0.92

VCDL range: 35 – 778 ps

Die Photo



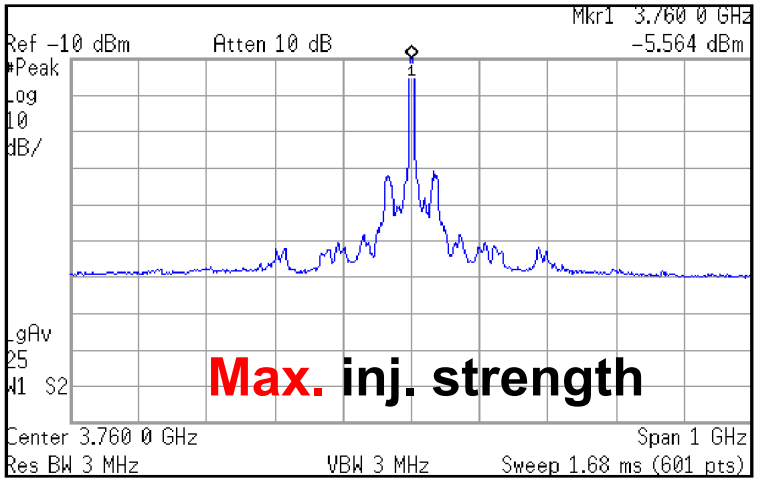
Core



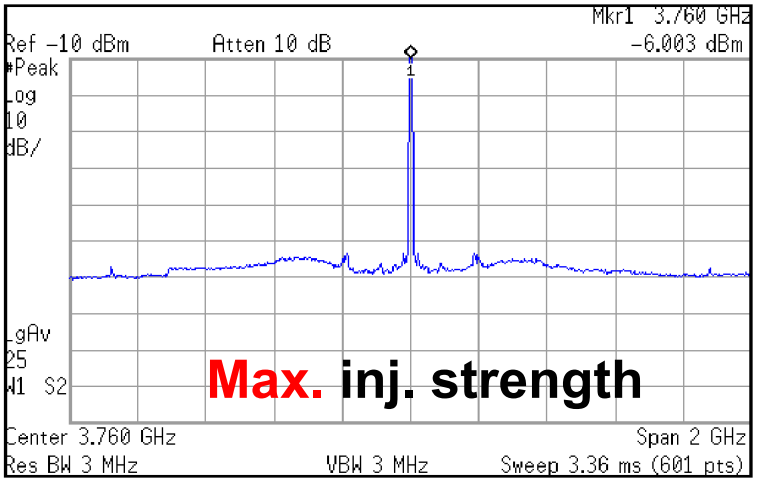
- 20nm CMOS
- VDD: 1.1/1.25V (including IR-drop)
- On-wafer probing

Case 1: N = 1, Fout = 3.7 GHz

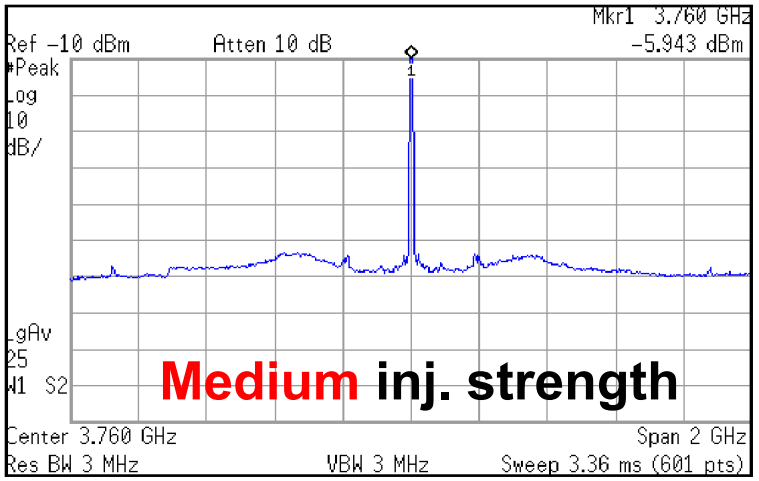
Injection-locked w/o PPM



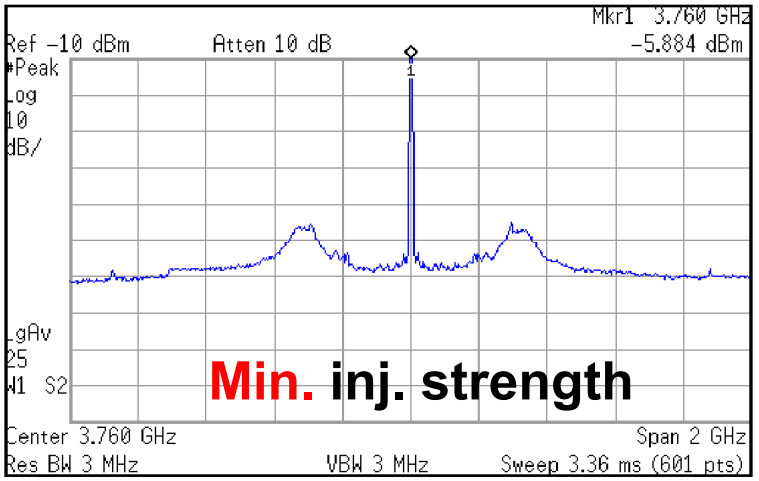
w/ PPM



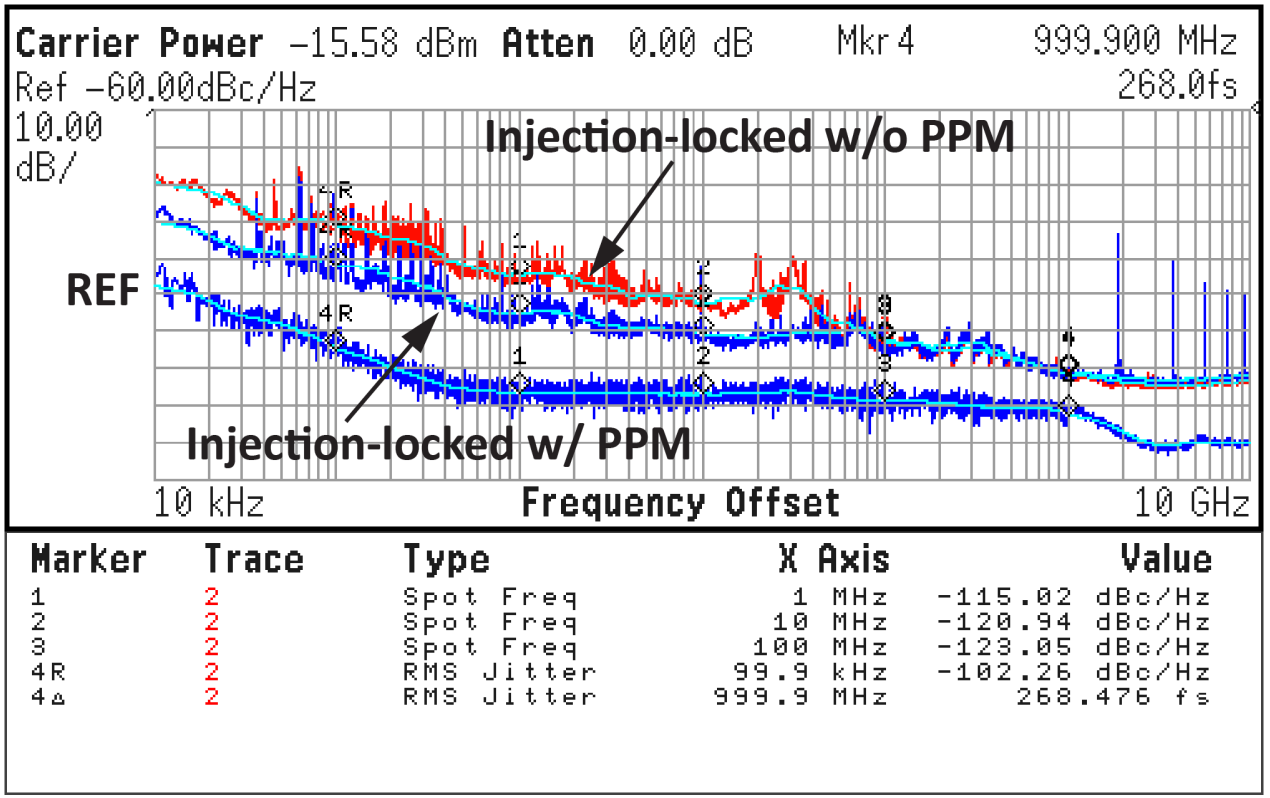
w/ PPM



w/ PPM



Case 2: N = 8, Fout = 15 GHz



Marker	Trace	Type	X Axis	Value
1	2	Spot Freq	1 MHz	-115.02 dBc/Hz
2	2	Spot Freq	10 MHz	-120.94 dBc/Hz
3	2	Spot Freq	100 MHz	-123.05 dBc/Hz
4R	2	RMS Jitter	99.9 kHz	-102.26 dBc/Hz
4Δ	2	RMS Jitter	999.9 MHz	268.476 fs

- **Integrated jitter (100kHz – 1GHz)**
  434fs w/o PPM vs. 268fs w/ PPM

Comparison

	This Work	[1]	[4]	[8]
Technology	20-nm CMOS	28-nm CMOS	90-nm CMOS	45-nm SOI
Implementation	PPM IL-Ring	LC-PLL / Ring-PLL	LC IL-PLL	Ring PLL
Freq. Range	2 – 16 GHz	8 – 13.1 GHz	20 ± 0.25 GHz	1.0 – 8.5 GHz
Output Freq.	15 GHz	13.1 GHz	20 GHz	2.5 GHz
Multiply Ratio (N)	8	N/A	8	25
Output Integrated RMS jitter	434 fs w/o PPM 268 fs w/ PPM (100 kHz – 1 GHz)	399 fs (sampling scope)	85 fs (100 Hz – 1 GHz)	990 fs (1 MHz – 1.25 GHz)
Reference Source Phase Noise	-136.6 dBc/Hz (10-MHz offset)	N/A	-150 dBc/Hz* (10-MHz offset)	N/A
Supply Voltage	1.25/1.1 V	1V/1.8V	1.5 V	2.5 V
Power Diss.	46.2 mW	N/A	105 mW	70 mW
Area	0.044 mm^2	0.12 mm^2	0.325 mm^2	N/A

*Estimated from paper

- **26.7% reduction compared to REF Jitter (= 366fs)**

Conclusions

- A PPM injection-locking technique is proposed for wideband reduction of VCO noise
- Measurements show a 60% improvement in integrated jitter with PPM enabled
- Small area allows for generation of independent low-jitter clocks for all channels

Acknowledgements

- Ying Shih, Gamal Said, Amy Chen, Kenny Hsieh, Fu-Tai An, Jalil Kamali, Daniel Wu, Jayesh Patil, and Kang-Wei Lai, Didem Turker, Ying Cao, Xilinx.

- Prof. Elad Alon and Yue Lu, UC Berkeley.

A Background Calibration Technique to Control Bandwidth in Digital PLLs

Giovanni Marzin*, Salvatore Levantino, Carlo Samori, Andrea L. Lacaita

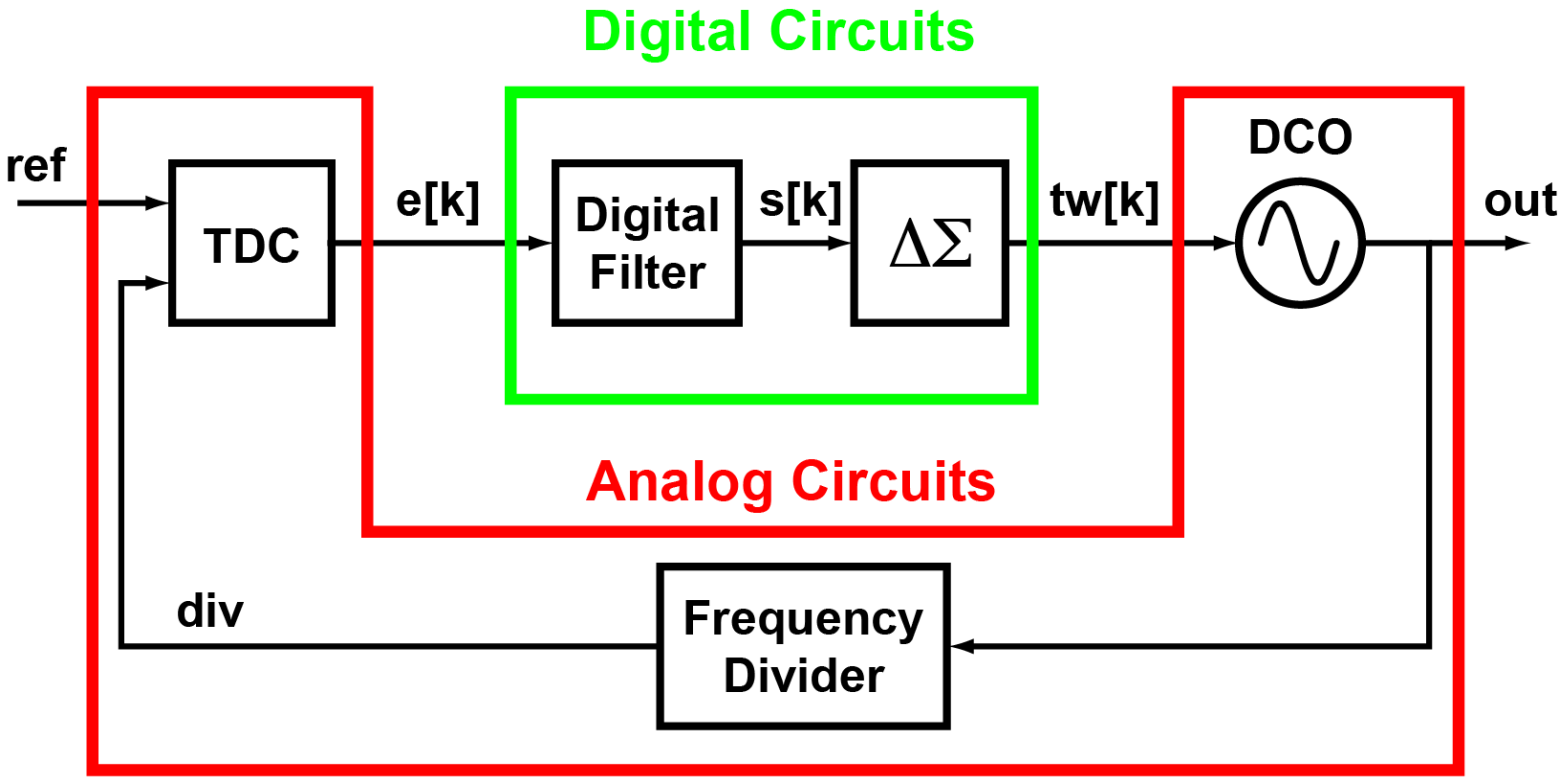
Politecnico di Milano, Milan, Italy

***Currently with BDL, Warren, NJ**

Motivation

- PLL BW directly affects performance:
  - settling time
  - stability margin
  - jitter vs power
- PLL BW inaccurate due to PVT variations
- Need accurate setting of PLL BW:
  - Without increasing jitter
  - Without increasing power consumption
  - Background calibration preferred

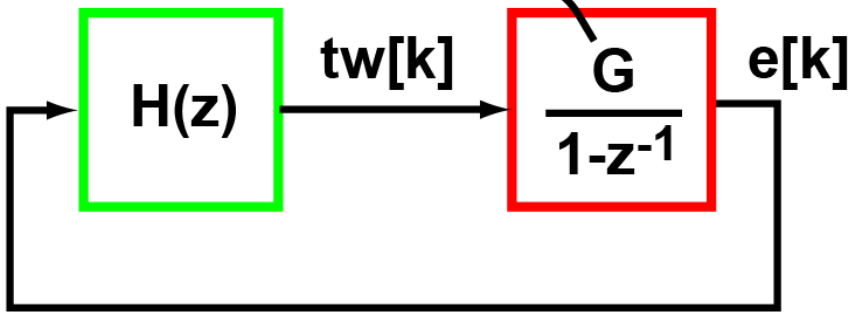
Typical Digital PLL



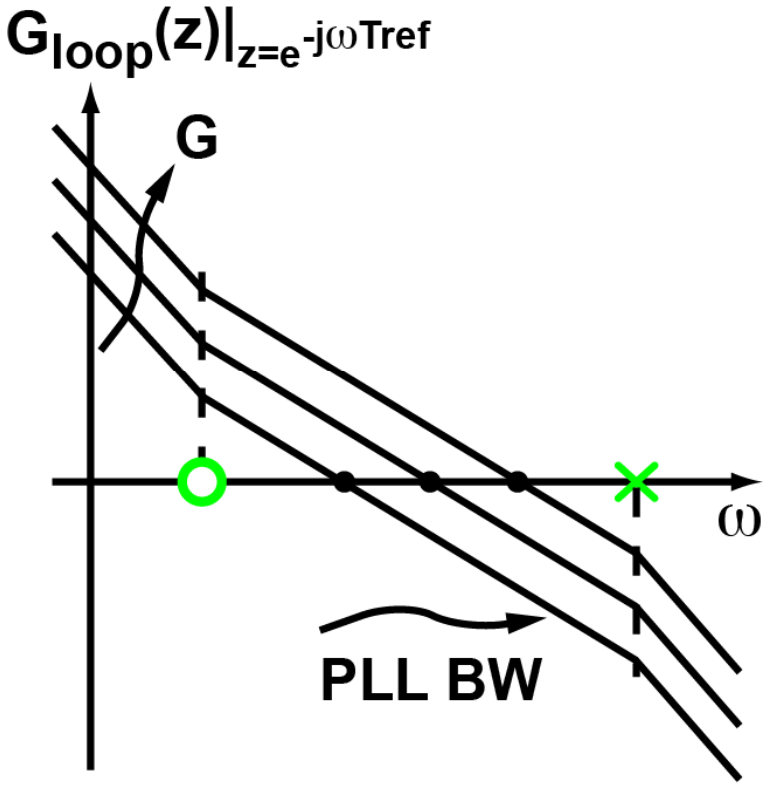
- Digital filter precisely sets PLL singularities
- Loop gain is a function of analog parameters

Loop Gain of Conventional DPLL

$$G = \frac{K_{tdc} K_{dco} T_{ref}}{N}$$

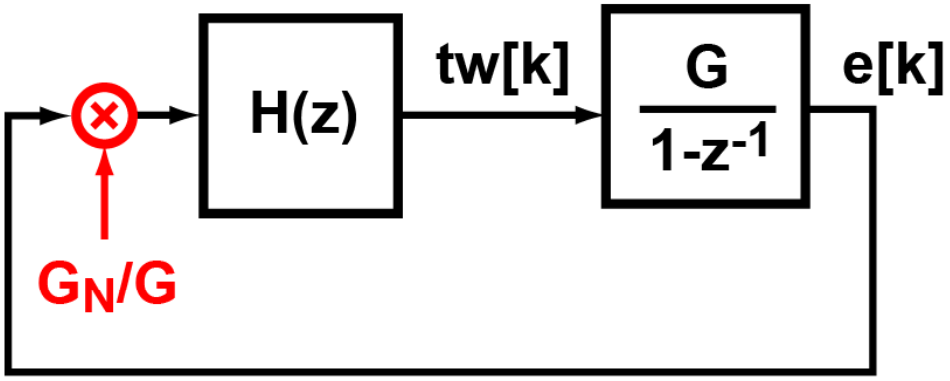


$$G_{loop}(z) = G \cdot \frac{H(z)}{1-z^{-1}}$$

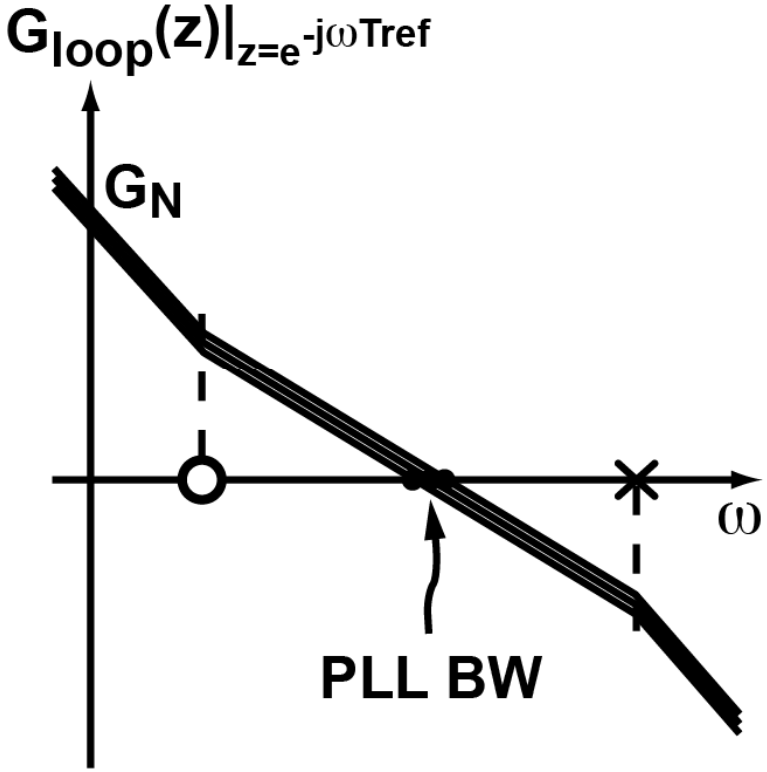


- Loop gain depends on PVT-sensitive parameters, such as TDC and DCO gain

Loop Gain Normalization



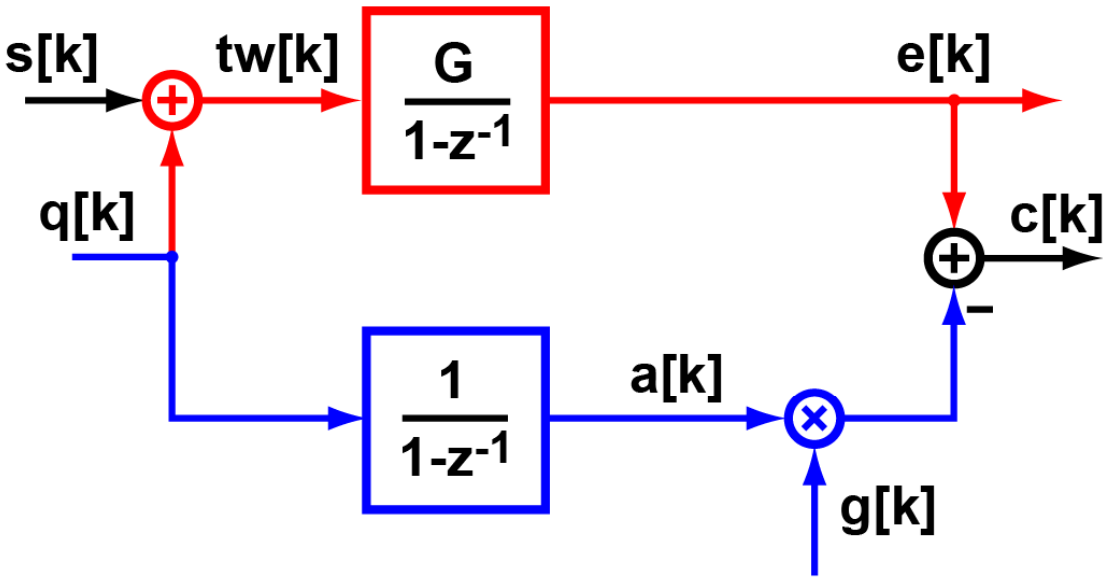
$$G_{loop}(z) = G_N \cdot \frac{H(z)}{1-z^{-1}}$$



- PLL BW becomes repeatable, since loop gain only depends on digital parameters

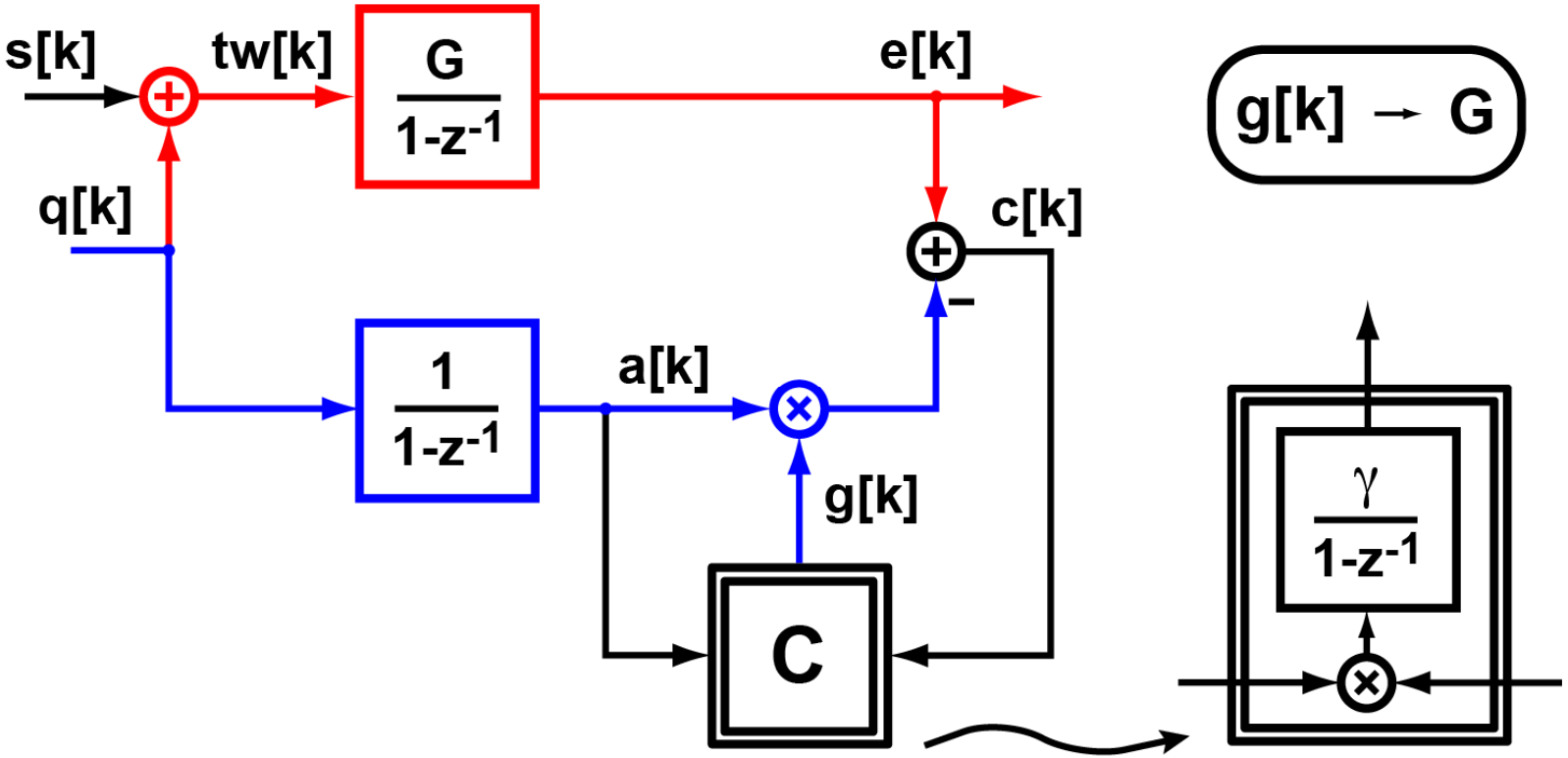
How can we automatically estimate the loop gain G?

Principle of Automatic-BW-Control (I)



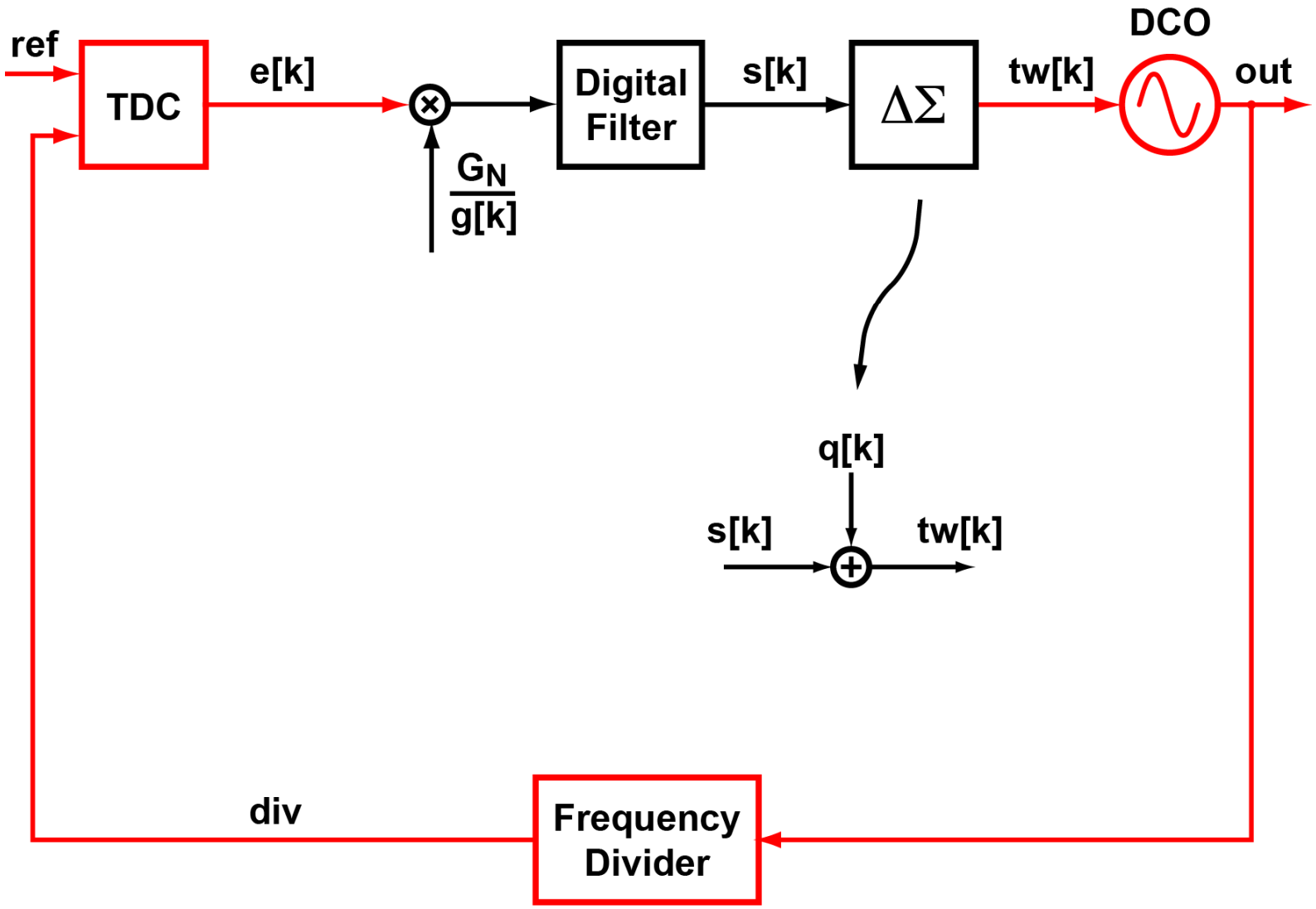
- Digital replica of analog section
- Training sequence q[k] to equalize the paths

Principle of Automatic-BW-Control (II)

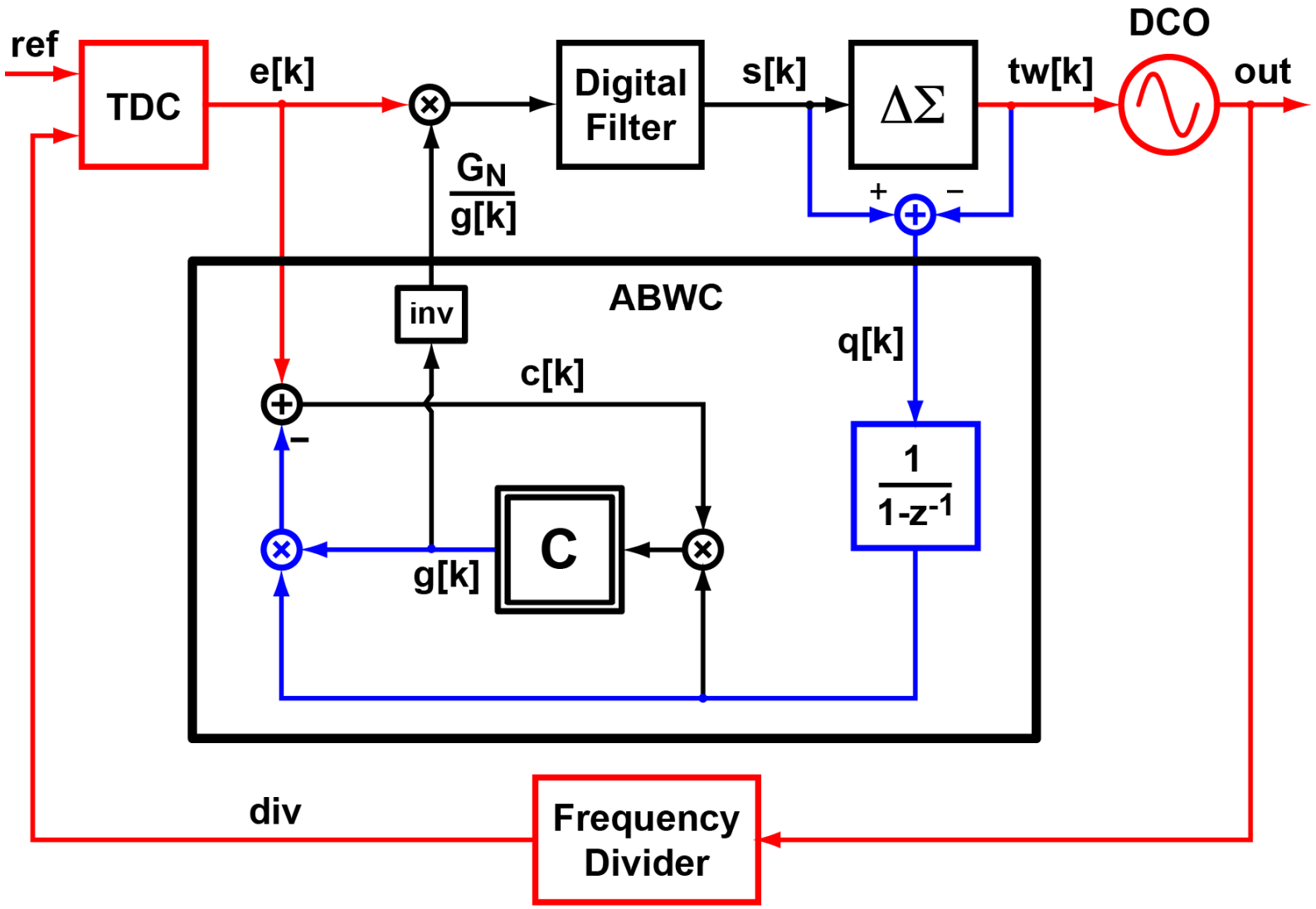


- Gains of the two paths equalized by feedback

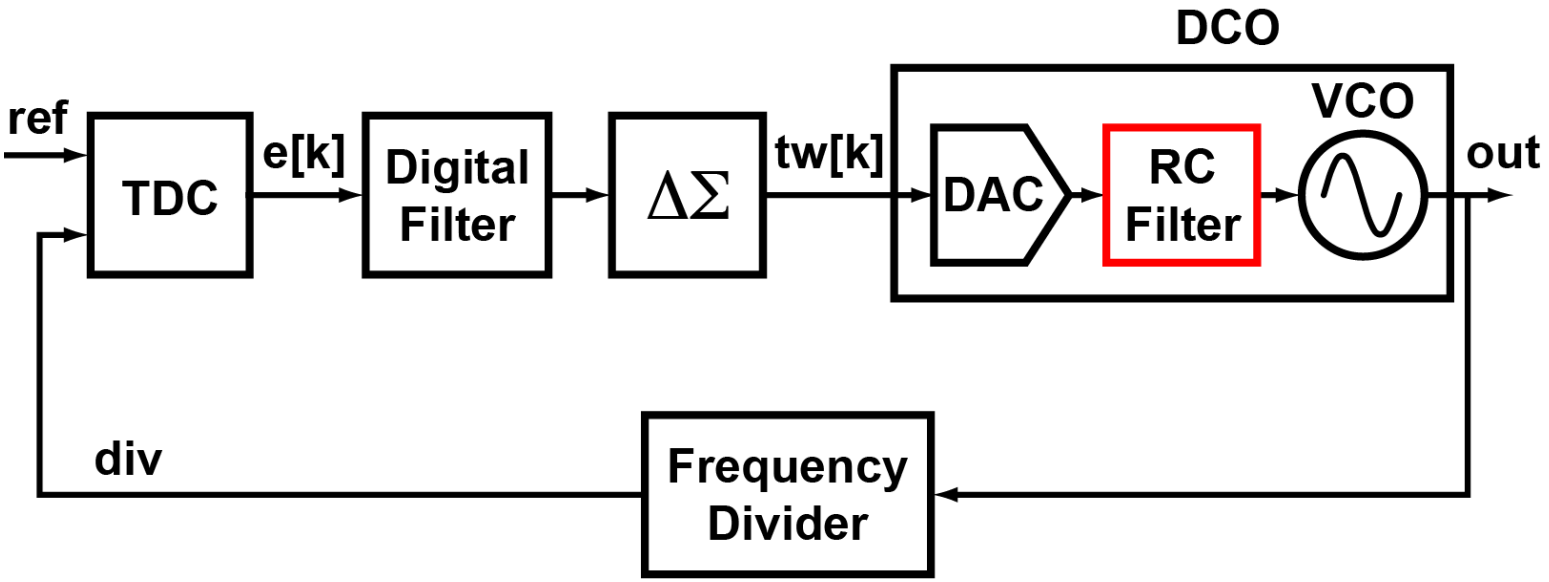
PLL with Bandwidth Calibration (I)



PLL with Bandwidth Calibration (II)



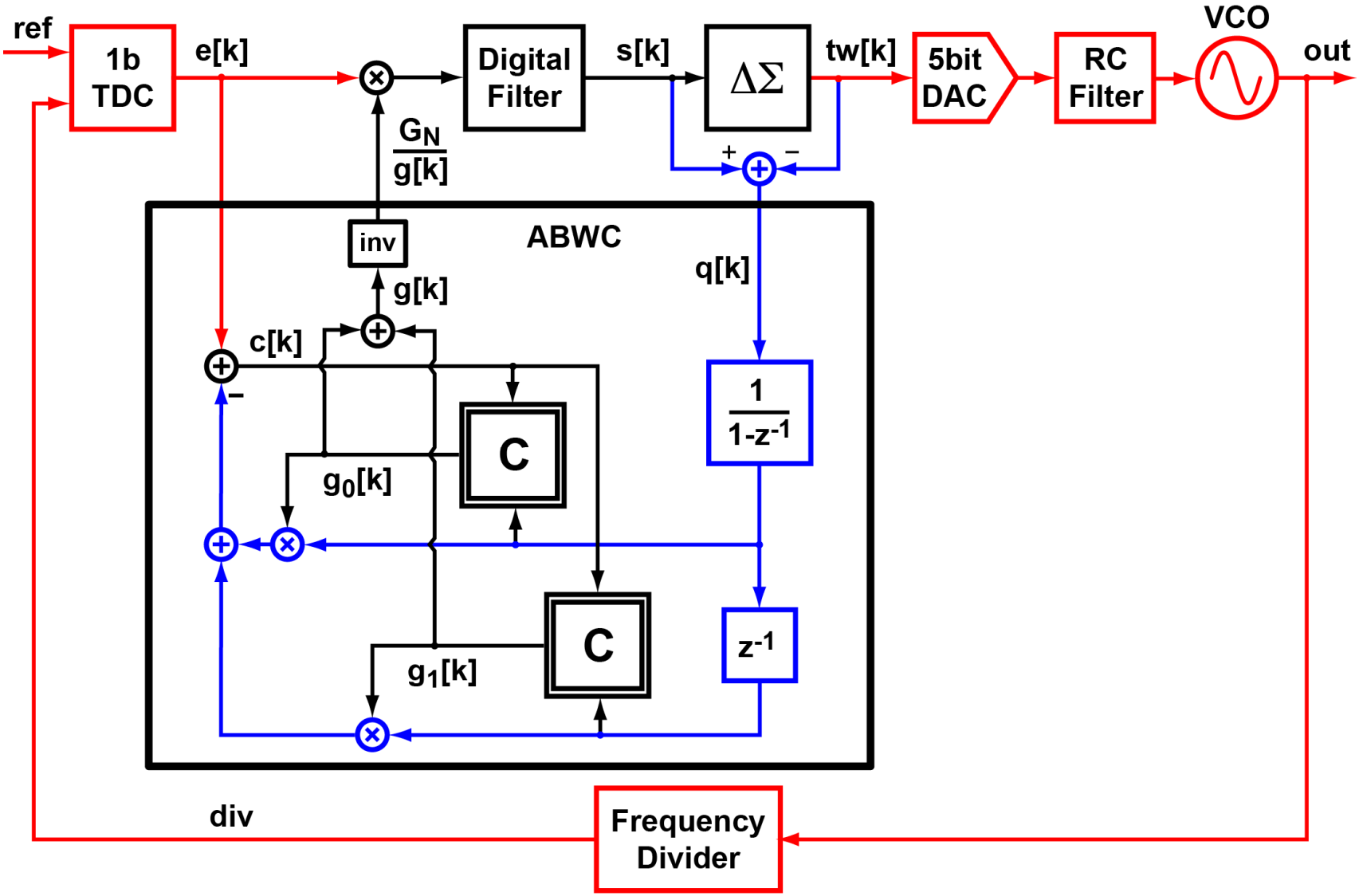
Digital PLL Conventional Implementation



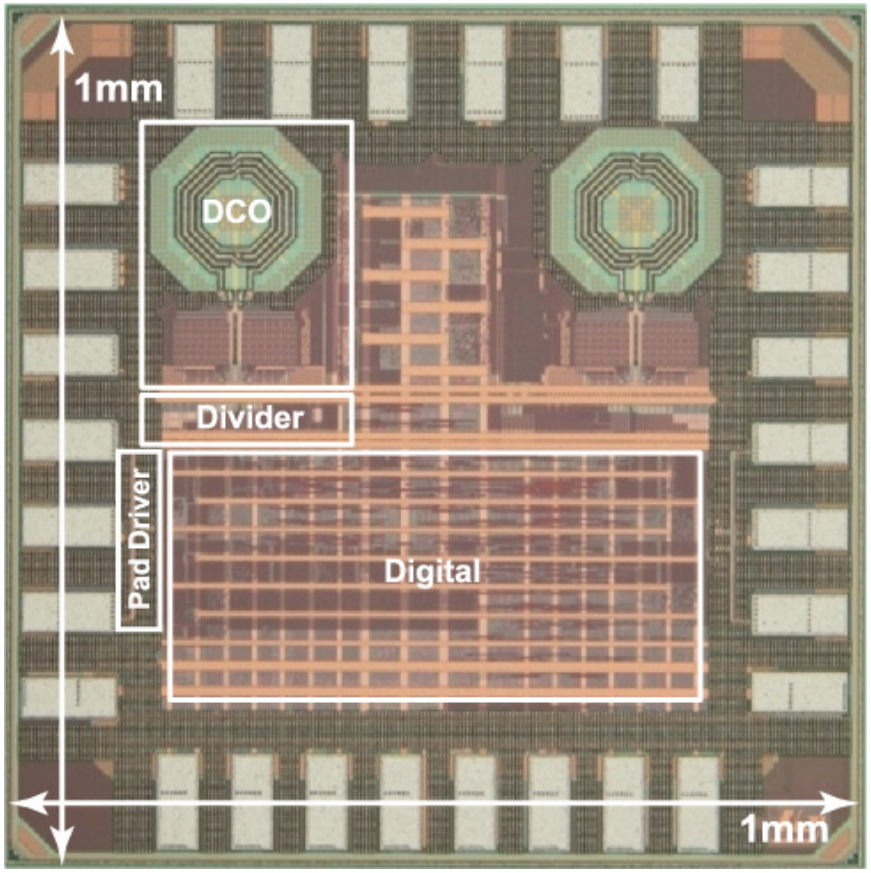
Hsu et al., ISSCC 2008

- An additional pole is typically introduced in the DCO transfer function
- The pole is placed beyond PLL BW to filter quantization noise

Proposed Digital PLL Architecture



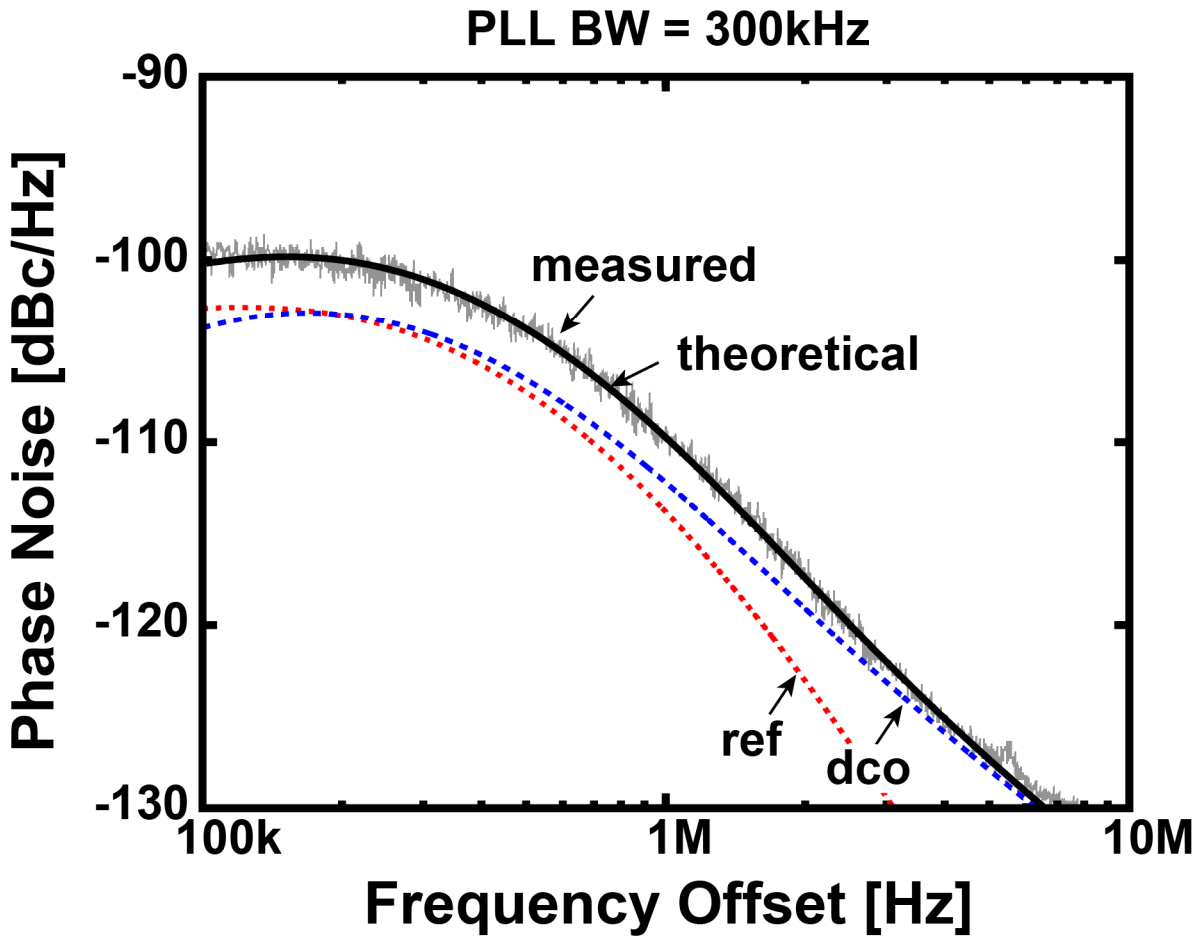
Die Photograph



- 65nm CMOS
- Active area: 0.2mm^2
- Supply voltage: 1.2V
- Power: 4.5mW
- Calibration loop dissipation: 0.04mW
- Frequency range: 3-4GHz

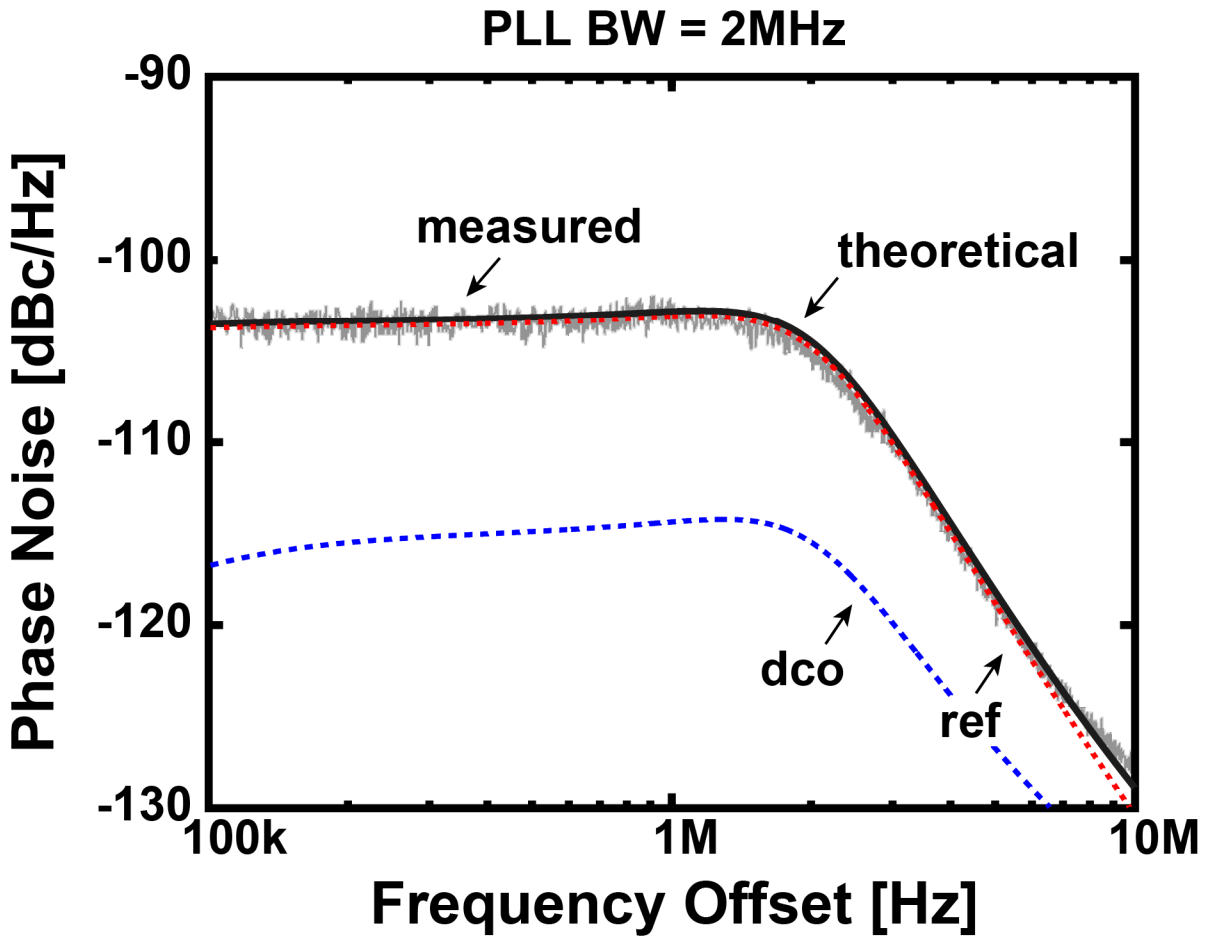
Measurement Results

Phase Noise at 300-kHz PLL BW



- Integrated jitter = 440 fs rms

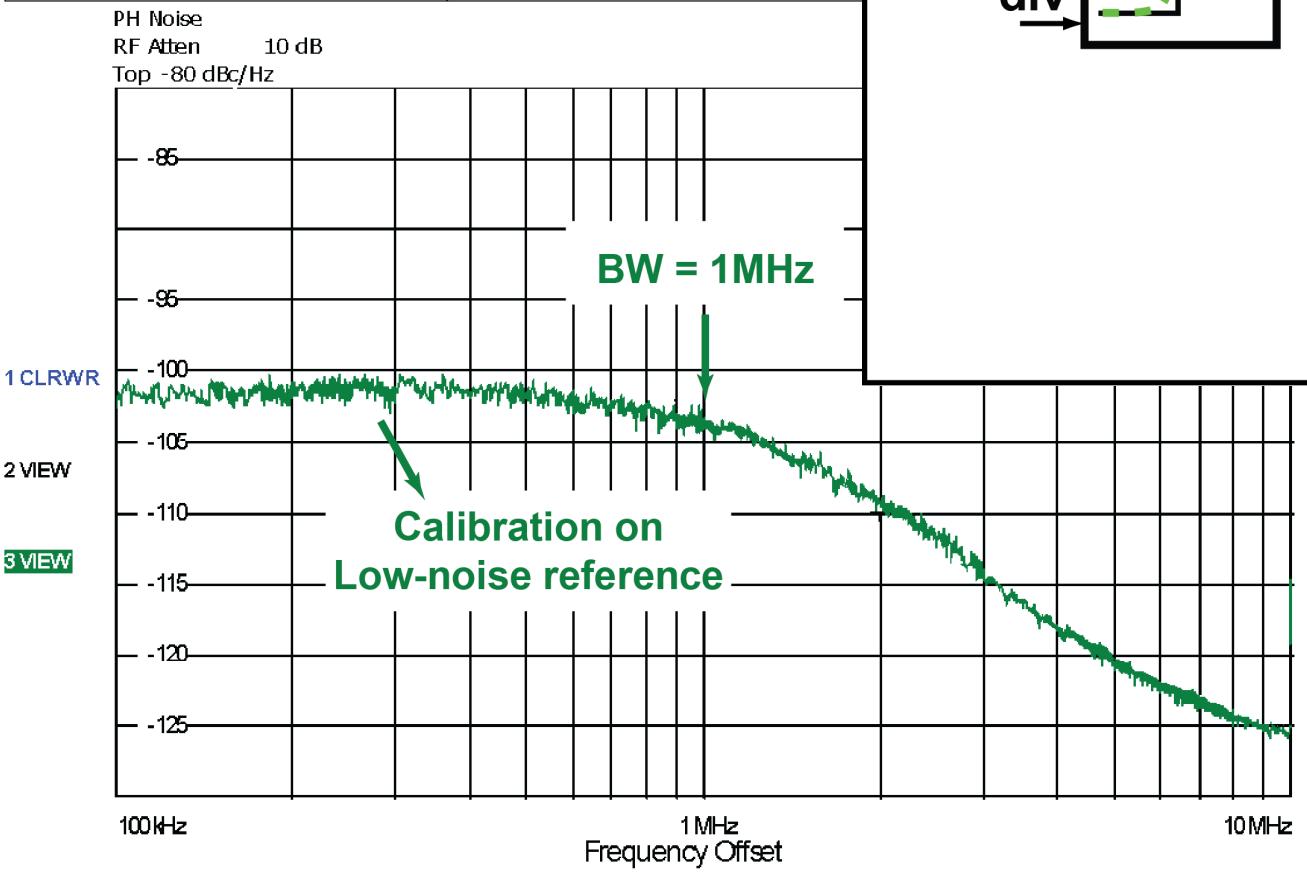
Phase Noise at 2-MHz PLL BW

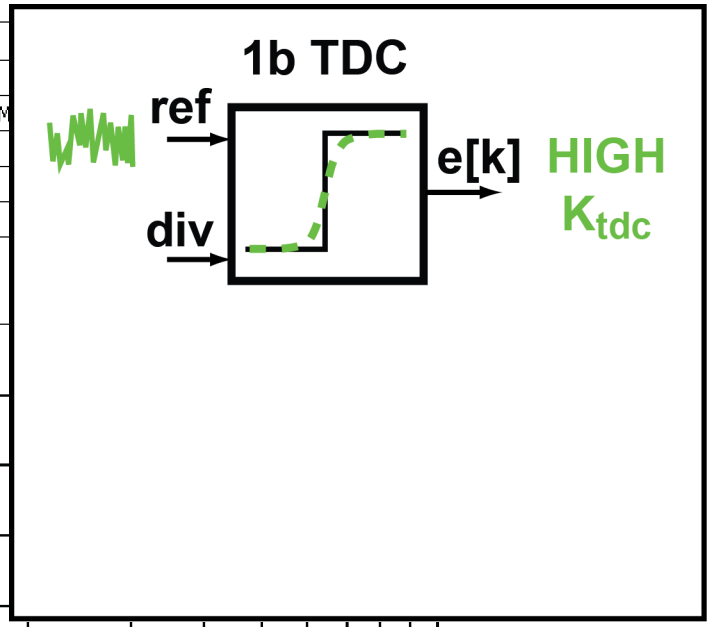


- Integrated jitter = 680 fs rms

Phase Noise at Low-Noise Ref

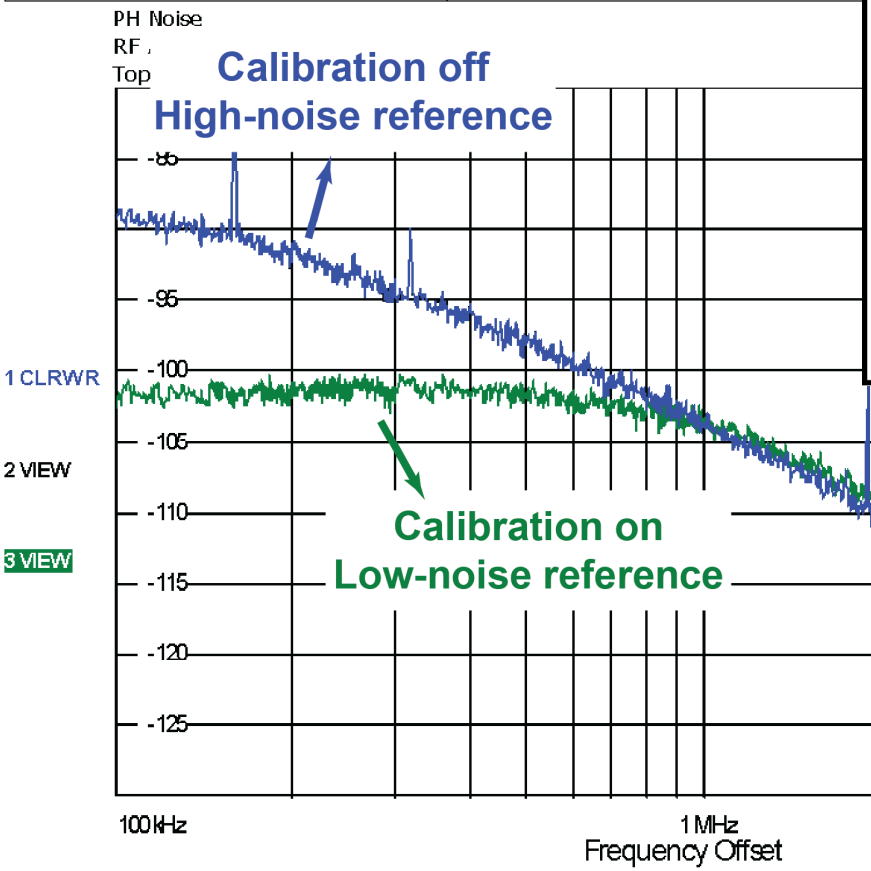
PHASE NOISE			
Settings		Residual Noise	
Signal Freq:	3.609994 GHz	Evaluation from 10 kHz	to 10 M
Signal Level:	-8.71 dBm	Residual PM	0.861 °
Signal Freq Δ:△	5.06 Hz	Residual FM	23.753 kHz
Signal Level Δ: △	-0.01 dBm	RMS Jitter	0.6628 ps

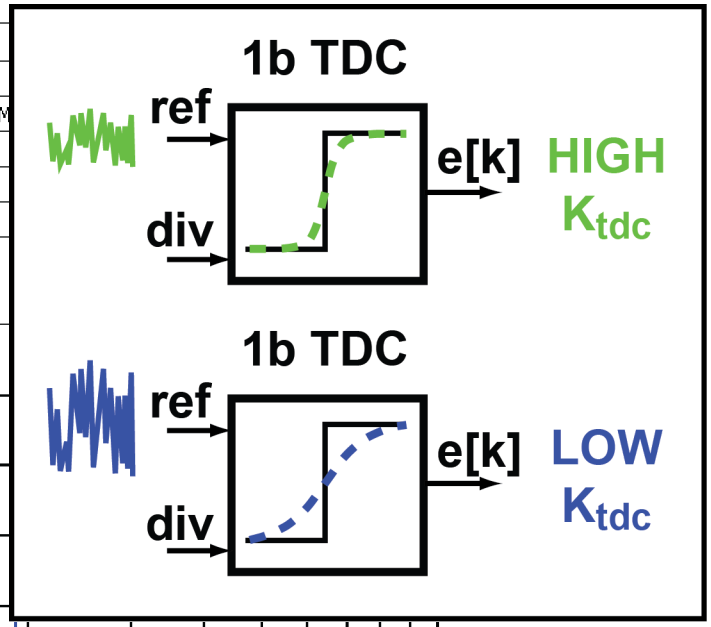




Phase Noise at High-Noise Ref w/o Cal

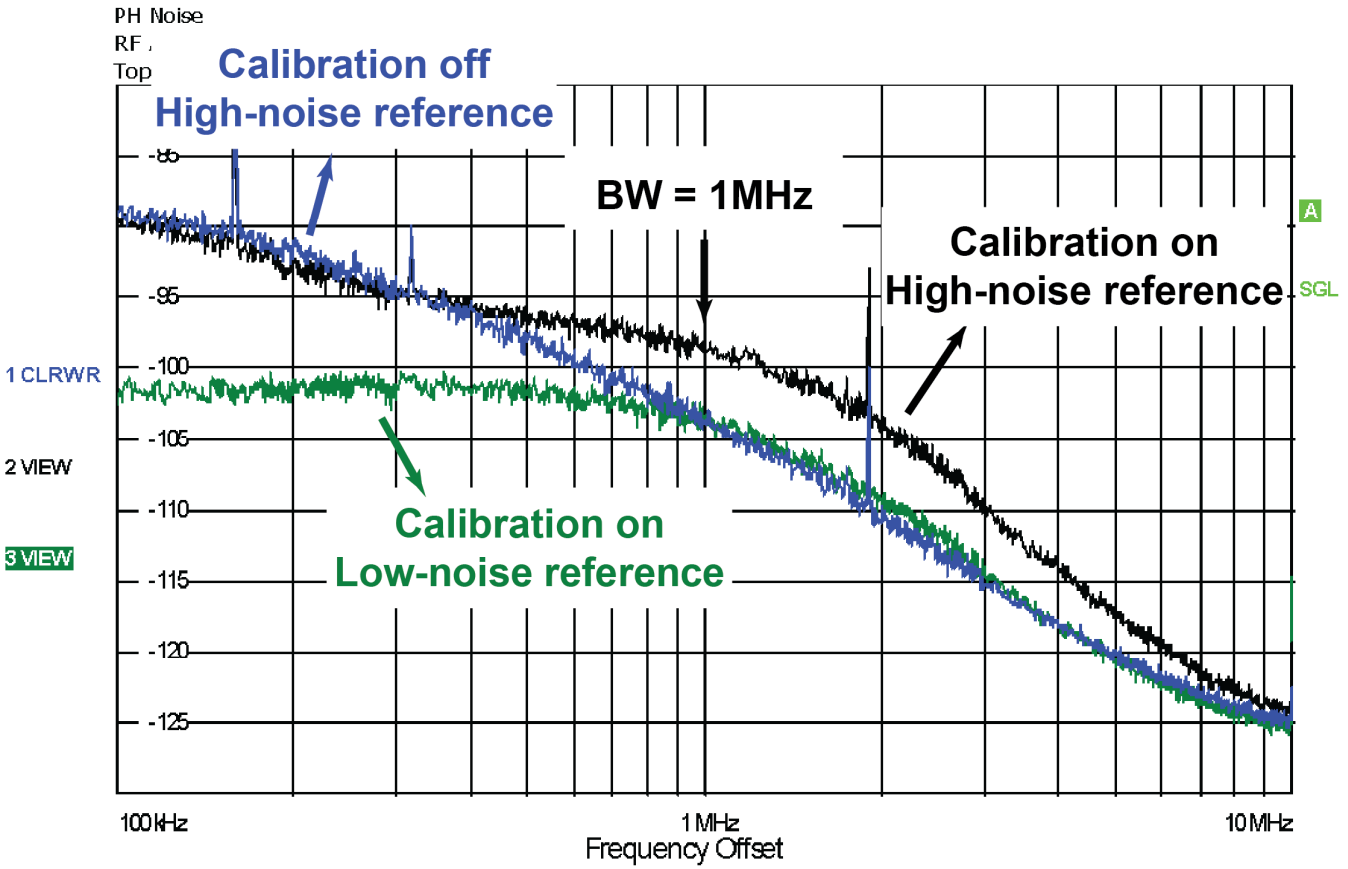
PHASE NOISE			
Settings		Residual Noise	
Signal Freq:	3.609994 GHz	Evaluation from 10 kHz	to 10 M
Signal Level:	-8.71 dBm	Residual PM	0.861 °
Signal Freq Δ:△	5.06 Hz	Residual FM	23.753 kHz
Signal Level Δ: △	-0.01 dBm	RMS Jitter	0.6628 ps





Phase Noise at High-Noise Ref with Cal

PHASE NOISE					
Settings		Residual Noise		Spot Noise [T3]	
Signal Freq:	3.609994 GHz	Evaluation from 10 kHz	to 10 MHz	1 kHz	** Not Valid **
Signal Level:	-8.71 dBm	Residual PM	0.861 °	10 kHz	** Not Valid **
Signal Freq Δ:△	5.06 Hz	Residual FM	23.753 kHz	100 kHz	-101.73 dBc/Hz
Signal Level Δ: △	-0.01 dBm	RMS Jitter	0.6628 ps	1 MHz	-103.65 dBc/Hz



Conclusions

- **High-accuracy low-power automatic bandwidth control of PLL obtained with:**
  - **Fully digital background calibration**
  - **$\Delta\Sigma$ error used as training sequence**
  - **Two-tap FIR filter estimation**

BW regulation: 100 kHz - 2 MHz
Accuracy: 4%
Jitter: 440 fs rms
Overall power: 4.5 mW